Coalescing Logistics (Again)

Rule

– When building the interference graph, do NOT make virtual registers interfere due to copies.
– If the virtual registers $s_1$ and $s_2$ do not interfere and there is a copy statement $s_1 = s_2$ then $s_1$ and $s_2$ can be coalesced.
– Example

\[
\begin{align*}
    a &= t + u \\
    \ldots \\
    b &= a \\
    c &= a \\
    \ldots \\
    x &= b + w \\
    z &= c + y
\end{align*}
\]

Before Coalescing

\[
\begin{align*}
    ab &= t + u \\
    \ldots \\
    c &= ab \\
    \ldots \\
    x &= ab + w \\
    z &= c + y
\end{align*}
\]

After Coalescing

Architectures with Callee and Caller Registers

Alpha

– 7 callee-saved out of 32 registers

MIPS

– caller-saved: $s0$-$s9$, $a0$-$a3$, $v0$-$v1$
– callee-saved: $s0$-$s7$, $ra$

PPC

– 18 callee-saved
– 14 caller-saved

StarCore EABI

– 4 callee-saved
– 28 caller-saved