

@article{Bao:2016:SDF:3012405.3011017, author = {Bao, Wenlei and Hong, Changwan and Chunduri, Sudheer and Krishnamoorthy, Sriram and Pouchet, Louis-Noël and Rastello, Fabrice and Sadayappan, P.}, title = {Static and Dynamic Frequency Scaling on Multicore CPUs}, journal = {ACM Trans. Archit. Code Optim.}, issue_date = {December 2016}, volume = {13}, number = {4}, month = dec, year = {2016}, issn = {1544-3566}, pages = {51:1-51:26}, articleno = {51}, numpages = {26}, url = {<http://doi.acm.org/10.1145/3011017>}, doi = {10.1145/3011017}, acmid = {3011017}, publisher = {ACM}, address = {New York, NY, USA}, keywords = {Affine Programs, CPU Energy, Static Analysis, Voltage and Frequency Scaling}, }

@inproceedings{Pouchet:2013:PDR:2435264.2435273, author = {Pouchet, Louis-Noël and Zhang, Peng and Sadayappan, P. and Cong, Jason}, title = {Polyhedral-based Data Reuse Optimization for Configurable Computing}, booktitle = {Proceedings of the ACM/SIGDA International Symposium on Field Programmable Gate Arrays}, series = {FPGA '13}, year = {2013}, isbn = {978-1-4503-1887-7}, location = {Monterey, California, USA}, pages = {29-38}, numpages = {10}, url = {<http://doi.acm.org/10.1145/2435264.2435273>}, doi = {10.1145/2435264.2435273}, acmid = {2435273}, publisher = {ACM}, address = {New York, NY, USA}, keywords = {compilation, data reuse, high-level synthesis, program transformations}, }

@article{Kong:2013:PTM:2499370.2462187, author = {Kong, Martin and Veras, Richard and Stock, Kevin and Franchetti, Franz and Pouchet, Louis-Noël and Sadayappan, P.}, title = {When Polyhedral Transformations Meet SIMD Code Generation}, journal = {SIGPLAN Not.}, issue_date = {June 2013}, volume = {48}, number = {6}, month = jun, year = {2013}, issn = {0362-1340}, pages = {127-138}, numpages = {12}, url = {<http://doi.acm.org/10.1145/2499370.2462187>}, doi = {10.1145/2499370.2462187}, acmid = {2462187}, publisher = {ACM}, address = {New York, NY, USA}, keywords = {affine scheduling, autotuning, compiler optimization, loop transformations, program synthesis}, }

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title      = "Minimizing the cost of iterative compilation with active  
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keywords   = "Active Learning, Compilers, Iterative Compilation, Machine  
Learning, Sequential Analysis;",  
author     = "William Ogilvie and Pavlos Petoumenos and Zheng Wang and Hugh  
Leather",  
note       = "Date of Acceptance: 25/10/2016",  
year       = "2016",  
month      = "10",  
booktitle  = "The International Symposium on Code Generation and Optimization  
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We describe the design of a convolutional neural network accelerator running on a Stratix V FPGA. The design runs at three times the throughput of previous FPGA CNN accelerator designs. We show that the throughput/watt is significantly higher than for a GPU, and project the performance when ported to an Arria 10 FPGA.

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{https://www.microsoft.com/en-us/research/publication/accelerating-deep-convolutional-neural-networks-using-specialized-hardware/}, address = {}, pages = {}, journal = {}, volume = {}, chapter = {}, isbn = {}, }
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location = {Monterey, CA, USA}, pages = {5-14}, numpages = {10}, url =
{http://doi.acm.org/10.1145/1950413.1950419}, doi = {10.1145/1950413.1950419}, acmid =
{1950419}, publisher = {ACM}, address = {New York, NY, USA}, keywords = {area, cmos, delay,
fpga, soft processor}, }
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author      = {Audrunas Gruslys and
               R{\'}{e}mi Munos and
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title       = {Memory-Efficient Backpropagation Through Time},
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journal    = {CoRR},  
volume     = {abs/1606.03401},  
year       = {2016},  
url        = {http://arxiv.org/abs/1606.03401},  
timestamp  = {Fri, 01 Jul 2016 17:39:49 +0200},  
biburl     = {http://dblp.uni-trier.de/rec/bib/journals/corr/GruslysMDLG16},  
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