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@ARTICLE{7738524, author={Y. H. Chen and T. Krishna and J. S. Emer and V. Sze}, journal={IEEE Journal of Solid-State Circuits}, title={Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks}, year={2017}, volume={52}, number={1}, pages={127-138}, keywords={DRAM chips;data flow computing;energy conservation;feedforward neural nets;learning (artificial intelligence);neural net architecture;power aware computing;reconfigurable architectures;AI systems;AlexNet;CNN shapes;DRAM accesses;Eyeriss;MAC;RS dataflow reconfiguration;accelerator chip;convolutional layers;data movement energy cost;dataflow processing;deep convolutional neural networks;energy efficiency;energy-efficient reconfigurable accelerator;multiply and accumulation;off-chip DRAM;reconfiguring architecture;row stationary;spatial architecture;Clocks;Computer architecture;Hardware;Neural networks;Random access memory;Shape;Throughput;Convolutional neural networks (CNNs);dataflow processing;deep learning;energy-efficient accelerators;spatial architecture}, doi={10.1109/JSSC.2016.2616357}, ISSN={0018-9200}, month={Jan},}

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Address = {New Delhi, India},
Author = {Rajopadhye, S. V. and Purushothaman, S. and Fujimoto, R. M.},
Booktitle = {Proceedings, Sixth Conference on Foundations of Software Technology and Theoretical Computer Science},
Key = {Rajopadhye86b},
Month = {December},
Pages = {488-503},
Publisher = {Springer Verlag, LNCS~241},
Title = {On Synthesizing Systolic Arrays from Recurrence Equations with Linear Dependencies},
Year = {1986}}

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Author = {Quinton, P. and {Van Dongen}, V.},
Journal = {Journal of {VLSI} Signal Processing},
Number = 2,
Pages = {95-113},

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title     = {Some Efficient Solutions to the Affine Scheduling Problem.
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journal   = {International Journal of Parallel Programming},
volume    = {21},
number    = {5},
year      = {1992},
pages     = {313-347},
ee        = {http://dx.doi.org/10.1007/BF01407835}

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journal   = {International Journal of Parallel Programming},
volume    = {21},
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title =      {Fuzzy Array Data Flow Analysis},
journal =    {Journal of Parallel and Distributed Computing},
year =      1997,

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volume =      40,  
number =      2,  
pages =       {210-226},  
month =       {Feb}}
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booktitle =    {Proceedings of the International Conference on Compiler  
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series =       {LNCS},  
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month =        Mar,  
publisher =    {Springer-Verlag},
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year={2011}, pages={35-42}, keywords={floating point arithmetic;matrix multiplication;GFLOPS-
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journal     = {CoRR},
volume      = {abs/1410.0759},
year        = {2014},
url         = {http://arxiv.org/abs/1410.0759},
timestamp   = {Sun, 02 Nov 2014 11:25:59 +0100},
biburl      =
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bibsource   = {dblp computer science bibliography, http://dblp.org}
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title={Synthesizing benchmarks for predictive modeling},

author={Cummins, Chris and Petoumenos, Pavlos and Wang, Zheng and Leather, Hugh},

year={2017},

url={<http://homepages.inf.ed.ac.uk/hleather/publications/2017-benchsynth-cgo.pdf>}

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title={Optimistic Loop Optimization},

author={Doerfert, Johannes and Grosser, Tobias and Hack, Sebastian},

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title = "Minimizing the cost of iterative compilation with active learning",

keywords = "Active Learning, Compilers, Iterative Compilation, Machine Learning, Sequential Analysis;",

author = "William Ogilvie and Pavlos Petoumenos and Zheng Wang and Hugh Leather",

note = "Date of Acceptance: 25/10/2016",


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year      = "2016",
month     = "10",
booktitle = "The International Symposium on Code Generation and Optimization
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Adrian M. and Chung, Eric S. and Chiou, Derek and Constantinides, Kypros and Demme, John and
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Michael and Hauck, Scott and Heil, Stephen and Hormati, Amir and Kim, Joo-Young and Lanka,
Sitaram and Larus, James and Peterson, Eric and Pope, Simon and Smith, Aaron and Thong, Jason and
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= {Minneapolis, Minnesota, USA}, pages = {13-24}, numpages = {12}, url =
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[download]

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= {Kalin Ovtcharov, Olatunji Ruwase, Joo-Young Kim, Jeremy Fowers, Karin Strauss, Eric Chung}, title
= {Accelerating Deep Convolutional Neural Networks Using Specialized Hardware}, booktitle = {},
year = {2015}, month = {February}, abstract = {

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We describe the design of a convolutional neural network accelerator running on a Stratix V FPGA. The design runs at three times the throughput of previous FPGA CNN accelerator designs. We show that the throughput/watt is significantly higher than for a GPU, and project the performance when ported to an Arria 10 FPGA.

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{https://www.microsoft.com/en-us/research/publication/accelerating-deep-convolutional-neural-networks-using-specialized-hardware/}, address = {}, pages = {}, journal = {}, volume = {}, chapter = {}, isbn = {}, }

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series = {ICS '01}, year = {2001}, isbn = {1-58113-410-X}, location = {Sorrento, Italy}, pages =
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Williams, Samuel and Straalen, Brian Van and Oliker, Leonid and Colella, Phillip}, title = {Compiler-
Directed Transformation for Higher-Order Stencils}, booktitle = {Proceedings of the 2015 IEEE
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{http://dx.doi.org/10.1109/IPDPS.2015.103}, doi = {10.1109/IPDPS.2015.103}, acmid = {2863932},
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`@inproceedings{Wong:2011:CFV:1950413.1950419, author = {Wong, Henry and Betz, Vaughn and Rose, Jonathan}, title = {Comparing FPGA vs. Custom Cmos and the Impact on Processor Microarchitecture}, booktitle = {Proceedings of the 19th ACM/SIGDA International Symposium on Field Programmable Gate Arrays}, series = {FPGA '11}, year = {2011}, isbn = {978-1-4503-0554-9}, location = {Monterey, CA, USA}, pages = {5-14}, numpages = {10}, url = {http://doi.acm.org/10.1145/1950413.1950419}, doi = {10.1145/1950413.1950419}, acmid = {1950419}, publisher = {ACM}, address = {New York, NY, USA}, keywords = {area, cmos, delay, fpga, soft processor}, }`

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author      = {Audrunas Gruslys and  
              R{\'}mi Munos and  
              Ivo Danihelka and  
              Marc Lanctot and  
              Alex Graves},  
title       = {Memory-Efficient Backpropagation Through Time},  
journal     = {CoRR},  
volume      = {abs/1606.03401},  
year        = {2016},  
url         = {http://arxiv.org/abs/1606.03401},  
timestamp   = {Fri, 01 Jul 2016 17:39:49 +0200},  
biburl      = {http://dblp.uni-trier.de/rec/bib/journals/corr/GruslysMDLG16},  
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`@inproceedings{FlowMap1994, author = {J. Cong and Ding, Yuzheng}, title = {FlowMap: an optimal technology mapping algorithm for delay optimization in lookup-table based FPGA designs}, booktitle = {IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems}, year = {1994}, isbn = {1937-4151}, pages = {1-12}, url = {http://ieeexplore.ieee.org/document/273754/}, doi = {10.1109/43.273754}, publisher = {IEEE} }`

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Elizabeth R. Jessup", keywords = "Community Earth System Model", keywords = "CESM Ensemble Consistency Test", keywords = "statistical consistency", keywords = "code modification as source of variability", keywords = "compiler as source of variability", keywords = "Community Atmosphere Model", keywords = "non-bit-for-bit", keywords = "Fused Multiply-Add" }

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