

@article{Bielecki:2016:TAN:3060371.3060383, author = {Bielecki, Włodzimierz and Pałkowski, Marek}, title = {Tiling Arbitrarily Nested Loops by Means of the Transitive}, journal = {Int. J. Appl. Math. Comput. Sci.}, issue_date = {12 2016}, volume = {26}, number = {4}, month = dec, year = {2016}, issn = {2083-8492}, pages = {919-939}, numpages = {21}, url = {<https://doi.org/10.1515/amcs-2016-0065>}, doi = {10.1515/amcs-2016-0065}, acmid = {3060383}, publisher = {Walter de Gruyter GmbH}, address = {Germany}, keywords = {iteration space slicing, polyhedral model, source-to-source compiler, tiling, transitive closure}, }

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@ARTICLE{7738524, author={Y. H. Chen and T. Krishna and J. S. Emer and V. Sze}, journal={IEEE Journal of Solid-State Circuits}, title={Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks}, year={2017}, volume={52}, number={1}, pages={127-138}, keywords={DRAM chips;data flow computing;energy conservation;feedforward neural nets;learning (artificial intelligence);neural net architecture;power aware computing;reconfigurable architectures;AI systems;AlexNet;CNN shapes;DRAM accesses;Eyeriss;MAC;RS dataflow reconfiguration;accelerator chip;convolutional layers;data movement energy cost;dataflow processing;deep convolutional neural networks;energy efficiency;energy-efficient reconfigurable accelerator;multiply and accumulation;off-chip DRAM;reconfiguring architecture;row stationary;spatial architecture;Clocks;Computer architecture;Hardware;Neural networks;Random access memory;Shape;Throughput;Convolutional neural networks (CNNs);dataflow processing;deep learning;energy-efficient accelerators;spatial architecture}, doi={10.1109/JSSC.2016.2616357}, ISSN={0018-9200}, month={Jan}, }

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Address = {New Delhi, India},
Author = {Rajopadhye, S. V. and Purushothaman, S. and Fujimoto, R.
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Key = {Rajopadhye86b},
Month = {December},
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Publisher = {Springer Verlag, LNCS~241},
Title = {On Synthesizing Systolic Arrays from Recurrence Equations
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Year = {1986}}
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    Journal = {Journal of {VLSI} Signal Processing},
    Number = 2,
    Pages = {95-113},
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    Title = {The Mapping of Linear Recurrence Equations on Regular
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    Volume = 1,
    Year = 1989}
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@Article{feautrier91, author= "Feautrier, P.", title= "Dataflow analysis of array and scalar
references", journal= "International Journal of Parallel Programming", year= 1991, volume= 20,
number= 1, pages= "23-53", month= "Feb", annote= "This article explains how a simple imperative
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    program (consisting only of assignments, for loops with affine loop
    limits, and arrays with affine index expressions), can be statically
    analyzed to find the flow dependencies."
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title     = {Some Efficient Solutions to the Affine Scheduling Problem.
             {Part I}. One-dimensional Time},
journal   = {International Journal of Parallel Programming},
volume    = {21},
number    = {5},
year      = {1992},
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author =      {Collard, J-F. and Barthou, D. and Feautrier, P.},  
title =       {Fuzzy Array Data Flow Analysis},  
journal =     {Journal of Parallel and Distributed Computing},  
year =        1997,  
volume =      40,  
number =      2,  
pages =       {210-226},  
month =       {Feb}}
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title =       {The Polyhedral Model Is More Widely Applicable Than You  
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booktitle =   {Proceedings of the International Conference on Compiler  
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year =        2010,  
series =      {LNCS},  
address =     {Paphos, Cyprus},  
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month =       Mar,  
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@INPROCEEDINGS{6043234, author={A. Pedram and A. Gerstlauer and R. A. v. d. Geijn},
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year={2011}, pages={35-42}, keywords={floating point arithmetic;matrix multiplication;GFLOPS-
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scaling;Bandwidth;Computer architecture;Hardware;Kernel;Linear algebra;Program
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@ARTICLE{7155440, author={T. Nowatzki and J. Menon and C. H. Ho and K. Sankaralingam}, journal={IEEE Micro}, title={Architectural Simulators Considered Harmful}, year={2015}, url={<http://ieeexplore.ieee.org/document/7155440/>}, volume={35}, number={6}, pages={4-12}, keywords={computer architecture;digital simulation;architectural layers;architectural simulators;black boxes;evaluation standard recalibration;quantitative simulators;Analytical models;Benchmark testing;Computer architecture;Market research;Mathematical model;Simulation;architecture;benchmarks;evaluation standards;footprint;modeling;simulators;validation}, doi={10.1109/MM.2015.74}, ISSN={0272-1732}, month={Nov},}

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               Philippe Vandermersch and
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journal     = {CoRR},
volume      = {abs/1410.0759},
year        = {2014},
url         = {http://arxiv.org/abs/1410.0759},
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{http://dblp.uni-trier.de/rec/bib/journals/corr/ChetlurWVCTCS14},
bibsource   = {dblp computer science bibliography, http://dblp.org}
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@inproceedings{Pouchet:2013:PDR:2435264.2435273, author = {Pouchet, Louis-Noel and Zhang, Peng and Sadayappan, P. and Cong, Jason}, title = {Polyhedral-based Data Reuse Optimization for Configurable Computing}, booktitle = {Proceedings of the ACM/SIGDA International Symposium on Field Programmable Gate Arrays}, series = {FPGA '13}, year = {2013}, isbn = {978-1-4503-1887-7}, location = {Monterey, California, USA}, pages = {29-38}, numpages = {10}, url = {<http://doi.acm.org/10.1145/2435264.2435273>}, doi = {10.1145/2435264.2435273}, acmid = {2435273}, publisher = {ACM}, address = {New York, NY, USA}, keywords = {compilation, data reuse, high-level synthesis, program transformations}, }

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@article{cummins2017synthesizing,

title={Synthesizing benchmarks for predictive modeling},

author={Cummins, Chris and Petoumenos, Pavlos and Wang, Zheng and Leather, Hugh},

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title      = "Minimizing the cost of iterative compilation with active
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keywords   = "Active Learning, Compilers, Iterative Compilation, Machine
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author     = "William Ogilvie and Pavlos Petoumenos and Zheng Wang and Hugh
Leather",
note       = "Date of Acceptance: 25/10/2016",
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Michael and Hauck, Scott and Heil, Stephen and Hormati, Amir and Kim, Joo-Young and Lanka,
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Xiao, Phillip Yi and Burger, Doug}, title = {A Reconfigurable Fabric for Accelerating Large-scale
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@miscellaneous{accelerating-deep-convolutional-neural-networks-using-specialized-hardware, author
= {Kalin Ovtcharov, Olatunji Ruwase, Joo-Young Kim, Jeremy Fowers, Karin Strauss, Eric Chung}, title
= {Accelerating Deep Convolutional Neural Networks Using Specialized Hardware}, booktitle = {},
year = {2015}, month = {February}, abstract = {

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We describe the design of a convolutional neural network accelerator running on a Stratix V FPGA. The design runs at three times the throughput of previous FPGA CNN accelerator designs. We show that the throughput/watt is significantly higher than for a GPU, and project the performance when ported to an Arria 10 FPGA.

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{https://www.microsoft.com/en-us/research/publication/accelerating-deep-convolutional-neural-networks-using-specialized-hardware/}, address = {}, pages = {}, journal = {}, volume = {}, chapter =
{}, isbn = {}, }

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series = {ICS '01}, year = {2001}, isbn = {1-58113-410-X}, location = {Sorrento, Italy}, pages =
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@article{DBLP:journals/corr/GruslysMDLG16,

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author      = {Audrunas Gruslys and  
              R{\'}mi Munos and  
              Ivo Danihelka and  
              Marc Lanctot and  
              Alex Graves},  
title       = {Memory-Efficient Backpropagation Through Time},  
journal     = {CoRR},  
volume      = {abs/1606.03401},  
year        = {2016},  
url         = {http://arxiv.org/abs/1606.03401},  
timestamp   = {Fri, 01 Jul 2016 17:39:49 +0200},  
biburl      = {http://dblp.uni-trier.de/rec/bib/journals/corr/GruslysMDLG16},  
bibsource   = {dblp computer science bibliography, http://dblp.org}
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