Switched Memory Architectures and the GRAIL

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Abstract

A Switched Memory Architecture (SMA) is a domain specific architecture designed for direct hardware implementation of a class of compute-intensive programs called Affine Control Loops (ACLs). An SMA is essentially, a multi-dimensional grid of processors or processing elements (PEs), each one consisting of (i) a functional unit that implements a data path to execute the operations in the loop body, (ii) a control unit and (iii) a set of memory banks to store the results of the computations. The PEs are interconnected through a special interconnection network called the GRAIL (Generic Reconfigurable Affine Interconnection Lattice). This talk describes the architecture, and our strategy for compiling loop programs to such a fabric.