Adaptive Models for Tile Size Selection

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Abstract

Tiling (or blocking) is widely used to exploit data locality and coarse-grained parallelism. Tile sizes significantly influence the performance and several models have been proposed for tile size selection. However, with advances in hardware and compiler optimizations, previous models are no longer effective. Developing efficient models each time the hardware or compiler changes require extensive time and effort of experts. We propose constructing such models by using machine learning techniques so that accounting for new processors/compiler features involve very little human effort. We show that our model for tile size selection, for programs optimized in the polyhedral framework of the IBM XLC, is fairly accurate in predicting good tile sizes and is better than previous models.