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Analysis of Bridging faults in Double BJT BiCMOS Circuit *

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Abstract

Combining the advantages of CMOS and bipolar, BiCMOS is emerging as a major technology for many high performance digital and mixed signal applications. Recent investigations have revealed that bridging faults can be a major failure mode in ICs. This paper presents effects of bridging faults in BiCMOS circuits. Bridging faults between logical units without feedback and logical units with feedback are considered. Several bridging faults can be detected by monitoring the power supply current (I_{DDQ} monitoring). Effects of bridging faults and bridging resistance on output logic levels have been examined along with their effects on noise immunity.

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1 Introduction

Combining the advantages of CMOS and Bipolar, BiCMOS is emerging as a major technology for many high performance digital and mixed signal applications. The main advantages of CMOS technology over bipolar are lower power dissipation and higher packing density. Bipolar technology offers better output current drive, switching speed, I/O speed and analog capability. Combining the advantages of bipolar and CMOS, BiCMOS offers the following advantages [1]; improved speed over CMOS, lower power dissipation compared to bipolar, flexibility in I/O (TTL, ECL, CMOS compatibility), high performance analog capability and latch up immunity. Compared to the CMOS counterparts, BiCMOS circuits can be faster by a factor of upto two for the same level of technology. Access times of less than 10ns have been reported for 0.8 μm BiCMOS ECL input/output 256K and 1M-bit SRAMs [2]. BiCMOS is even being considered for high performance microprocessors and dynamic RAMs, and it is felt that it will be one of the main technologies to drive almost all functions in the decade ahead [3].

Most of the defects and failures in present day integrated circuits can be abstracted to shorts and opens in the interconnects and degradation of devices [4]. Transistor level shorts and opens model many of the physical failures and defects in ICs [5]. A study by Galiay [6] on 4-bit MOS microprocessor chips revealed that many of the faults were shorts and opens at the transistor level. Analysis of faults in elementary static storage elements suggest that transistor level testing provides a higher coverage of faults compared to that at the gate level [7]. Thus, it is necessary to study the effects of failures at the transistor level and develop accurate fault models at this level [5]. The major fault models at transistor level are stuck-at faults, and shorts and opens of transistors and interconnects [8]. It has been shown [9] that the stuck-at model does not cover many of the manufacturing defects in BiCMOS devices and that most open faults manifest themselves as delay faults.

Rapid advances, increasing complexities and shrinking device geometries in VLSI have enabled complex integrated circuits to be manufactured for extremely complex systems at lower costs. Various modes of failures can occur in such complex VLSI devices, where bridging faults have been shown to be about half of the faults in CMOS circuits [10]. Another study [11], based on layout level defects using statistical data from fabrication process concludes that bridging faults can be upto 30% of all faults. Hence, bridging is an important failure mode which needs careful and systematic analysis. Bridging faults have long been regarded as a possible failure mode in digital systems [12, 13, 14]. Detailed examinations of bridging faults in nMOS/CMOS have been presented in [15, 16]. Effects of stuck-on and open of transistors in ECL OR/NOR gate and 2-level complex ECL gates were presented in [17, 18]. Bridging faults can occur

Figure 1: A D-BJT BiCMOS Nand.

within an integrated circuit or a printed circuit board during manufacturing or at a later stage. Most of the literature on bridging faults assumes a simple gate level model.

The most common type of BiCMOS circuits employ bipolar transistors to perform the function of driving output loads and CMOS to perform logic functions. In this paper, we briefly review the operation of a double BJT (D-BJT) BiCMOS NAND device. In this paper, we present the effects of bridging faults and bridging resistances on output logic levels and device current (I_{DDQ}) is examined along with their effects on noise immunity.

This paper is organized as follows. The operation of a basic BiCMOS NAND is explained in section 2. Section 3 deals with bridging within a logic element. Sections 4 and 5 cover bridging of logical nodes without feedback and with feedback respectively. Finally, conclusions drawn from the study are given in section 6.

2 D-BJT BiCMOS device

A Double BJT BiCMOS NAND realization is shown in Figure 1. The functioning of the BiCMOS NAND can be explained by first applying logic '0' to one or both of the inputs which would cause at least one P-device to be ON and at least one N-device in each serial N-pairs to be OFF. With at least one N-device in each serial N-pairs being OFF, no current is supplied to the base of Q_2 resulting in transistor Q_2 being OFF. With the P-devices (P_1 and/or P_2) ON, the base of the bipolar NPN transistor would be about 5V supplying base current and turning ON the bipolar transistor providing logic '1' at the output. With either of the inputs being at logic '0' and the other input at logic '1' would still cause either of the parallel connected P-devices to be ON and either of the series connected N-devices to be OFF. This would still supply base current to the bipolar transistor Q_1 causing logic '1' at the output. With both the inputs at logic '1', the P-devices (P_1 and P_2) would be turned OFF, and the N-devices N_1, N_2, N_3 and N_4 would be turned ON, supplying base current to Q_2 which discharges the load. Transistor N_1 and N_2 draw current from the base of Q_1 thus rapidly turning this device OFF. This will cause the output to be a logic '0'. Thus the circuit realizes the NAND function. It may be noted that the static power consumption of the circuit is negligible neglecting reverse biased leakage currents. A D-BJT BiCMOS gate consists of CMOS p- and n-parts to perform logic function, and two output BJTs for driving the output node.

D-BJT BiCMOS devices do not have the full V_{DD} to Ground logic swing of CMOS devices. The output High voltage (V_{OH}) is limited to V_{DD}-$V_{BE(Q1)}$ and output Low voltage (V_{OL}) is limited to V_{DD}-$V_{BE(Q2)}$. V_{ILmax} and V_{IHmin} were determined to be 2.2V and 2.7V respectively, by finding the $\frac{dV_{out}}{dV_{in}}$ = -1 points [19, 20] on the voltage characteristics. The logic levels for BiCMOS are 0.6V to 2.2V for logic level '0' and 2.7V to 4.4V for logic level '1' [21]. Any voltage between 2.2V and 2.7V is considered indeterminate. The device characteristics given for Fujitsu BiCMOS gate array devices [22] are V_{IHmin}=2V, V_{OHmin}=2.4V, V_{ILmax}=0.8V and V_{OLmax}=0.5V.

Major causes of bridging faults are related to the manufacturing defects. In the photolithography stages of the manufacturing process, diffraction and proximity are the prime source of excess metal causing bridging faults. Impurities and diffusion of metal are other sources responsible for such faults. Effects of input and output bridging faults in BiCMOS devices are examined for hard bridging as well as bridging with varying resistances. The following definitions are used in this paper.

Figure 2: D-BJT BiCMOS output bridging fault (Hard short).

3 Bridging within a logic element

Bridging faults within nMOS and CMOS logic elements were examined in [23]. Some bridging faults exhibit the same effect as stuck on faults [24]. It has been shown [6, 23] that nodes in a complex gate do not directly correspond to the nodes in an equivalent logic network and have shown examples of bridging faults that cannot be modelled directly at the gate level.

Bridging faults in bipolar devices have been considered in [8, 25, 26]. Shorts in TTL devices result in stuck at '0', '1' or are undetectable. Shorts in TTL NAND and CECL full adders were examined in [8]. An example [6] of a short within a complex gate which is impossible to model by conventional modelling was shown. While some of the bridging faults considered in this class result in non-logical output levels, others result in logic '0' and logic '1'. The overall effect of such bridging is to alter the function of the logic element.

4 Bridging of logical nodes without feedback

In this class of bridging faults, bridging of logical input and output nodes of logic elements are considered. Bridging can be either hard bridging or the bridging can exhibit significant resistance. The effects of bridging under hard bridging and for bridging with significant resistance are given in this section for D-BJT BiCMOS devices.

Figure 3: D-BJT BiCMOS output bridging fault (Hard short).

4.1 Hard bridging faults in D-BJT BiCMOS

In this subsection we assume hard shorts for bridging faults under consideration. In CMOS, the effects of bridging can be modelled by taking into account the resistances of the paths and bridging connections [15]. Consider a hard short between two D-BJT BiCMOS output inverters as shown in Figure 2. When the logic levels at nodes V_1 and V_2 are same, i.e., 00 or 11, then there is no direct path from V_{DD} to ground and hence, the same logic levels, i.e., 00 or 11, are maintained. Considering the case when one of the nodes is at logic level high (1) and the other node is at logic level low (0). A path is created between V_{DD} and ground leading to enhanced I_{DDQ}. Such output bridging faults in BiCMOS can be detected using power supply current monitoring (I_{DDQ} monitoring).

Since a hard short is assumed for the bridging fault, voltage levels appearing at node V_1 is the same as the voltage level appearing at node V_2 ($V_1 = V_2$). Consider the condition where V_1 is at logic level '1' (transistor Q_1 ON) and V_2 is at logic level '0' (transistor Q_2' ON). With the output bridging fault under consideration and since the parameters of transistors Q_1 and Q_2' are the same, the output settles at one-half of the output high ('1') logic level ($V_{OH}/2 = \approx 2.2$V), for input vectors A B = 0 1 and 1 0 as shown in Figure 3. Since there is a direct path from V_{DD} to ground, enhanced I_{DDQ} values are observed for output hard bridging faults. Here, current monitoring (I_{DDQ}) techniques can be implemented to detect such faults.

In a multilevel network, an input bridging fault can be analyzed similarly by considering the bridging

Figure 4: D-BJT BiCMOS output bridging fault (with significant resistance).

fault to be output bridging fault of the previous level.

4.2 Output bridging with varying resistances

Since bridging is not a deliberate feature, it may not always be a hard short and in general may exhibit a significant resistance. A very high resistance may imply a bridging fault of no consequence. The range of values exhibiting significant impact on the logic values is investigated.

Consider the two BiCMOS output stages as shown in Figure 4 with unknown bridging resistance R_X. When the logic levels at V_1 and V_2 are same, i.e., 00(11), then there is no direct path from V_{DD} to ground, leading to the same logic levels, i.e., 00(11) being maintained at V_1 and V_2. When one of the nodes is at logic level 'High' (1) and the other node is at logic level 'Low' (0) with a bridging resistance of a significant value ($R_X > 0\Omega$), the output logic levels at V_1 and V_2 needs to be studied.

Spice simulation of the BiCMOS output bridging fault was done for varying bridging resistances (R_X) and the output logic levels for both the nodes V_1 and V_2 plotted are shown in Figure 5. The inference drawn from this simulation is as follows:

(1) Node V_1 and V_2 remain at $\approx V_{OH}/2$ ($\approx$2.2V) for bridging resistance $R_X < \approx 3\Omega$. Output level of $\approx$2.2V is classified as logic level '0' for BiCMOS devices. However, the nodes V_1 and V_2 exhibit degraded noise immunity for these bridging resistances.

(2) Node V_2 remains at logic level '0' for all bridging resistances. However, noise immunity of the node V_2 is degraded for lower bridging resistance values.

Figure 6: Current [$i(V_{DD})$] vs. bridging resistance for output bridging faults.

Figure 7: Noise immunity of node V_2 under S-BJT BiCMOS output bridging fault.

(3) For bridging resistances $\geq\approx 3\Omega$ and $\leq\approx 40\Omega$, the logic level for node V_1 is in the 'Undefined' level. Though the output logic level is in the 'Undefined' level, current monitoring can be used to detect this bridging.

(4) When bridging resistance is greater than $\approx 40\Omega$, the bridging is of no consequence at the logic level.

In Emitter Coupled Logic devices using bipolar transistors, an undefined logic level input to a successive stage may cause an 'undefined' voltage level to appear at the output [27]. In nMOS/CMOS devices, the 'Undefined' level is interpreted by the successive stage as either a '1' or '0' depending on the logic threshold. As in nMOS/CMOS devices, the successive stage of a BiCMOS device employing both bipolar and CMOS devices interprets an undefined level as either a '1' or '0' depending on the logic threshold. Figure 6 shows the current [i(V_{DD})] drawn by the devices for varying bridging resistances.

Estimation of noise immunity for both the nodes were carried out. The voltage level obtained at the two nodes (V_1 and V_2) under varying bridging resistances were obtained. Noise immunity for 'High' logic level was estimated by computing the difference between the node voltage and V_{IHmin} (Minimum input voltage for logic level 'High'). Similarly, noise immunity for 'Low' logic level was estimated by computing the difference between V_{ILmax} (Maximum input voltage for logic level 'Low') and the node voltage.

Node V_2 remains at logic level 'L' irrespective of the bridging resistance. The noise immunity of this node is lightly degraded at low bridging resistances. Figure 7 shows noise immunity for node V_2 under

Figure 8: Noise immunity of node V_1 under S-BJT BiCMOS output bridging fault.

'Low' logic level conditions. Degraded noise immunity at low bridging resistance can be seen in Figure 7. As the output bridging resistance increases, the noise immunity of node V_2 increases. Figure 8 shows noise immunity for node V_1 under 'High' logic level condition. It can be seen that under high bridging resistances, the logic level stays on the correct side (logic level 'H'). As the value of the bridging resistance is lowered ($\approx 40\Omega$), the noise immunity of the node V_1 for logic level 'High' keeps getting lower until noise immunity becomes zero. Further lowering the value of bridging resistance causes the node V_1 to be at an undefined level. Continuing the process of lowering the value of the bridging resistances (below $\approx 3\Omega$) results in logic level 'Low' at the node V_1 which is a faulty logic level with a very low noise immunity ($\approx$0.006V), hence cannot be seen on the plot. A logic device being driven by this node may interpret this faulty logic level correctly.

5 Bridging of logical nodes with feedback

This class of bridging faults deals with logical nodes deriving its logic value from another due to bridging. If the feedback loop does not contain clocked storage elements, then asynchronous feedback paths are frequently introduced transforming combinational block into an asynchronous sequential circuit. It has been shown that if a feedback loop contains an odd number of inversions, then oscillations can occur [28]. The anomalous behavior seen in this class of bridging faults depends on propagation delay, rise time, fall

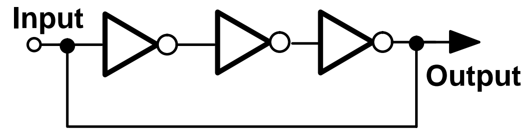

Figure 9: Feedback bridging across odd number of D-BJT BiCMOS inverters.

time as well as analog transfer characteristics of the bipolar transistors used in the device.

To analyze bridging faults of this class, consider a combinational block with inputs $A_1 \ldots A_n$ and outputs $Z_1 \ldots. Z_m$. Consider that input A_1 is bridged with output Z_1 through a sufficient bridging resistance (R_X). Assuming that an input vector is applied under which there is a sensitized path from A_1 to Z_1 through an odd number of inversions. When A_1 is logic level '1', Z_1 is '0' without feedback bridging. The situation will be different in the presence of feedback bridging. Considering the case when rise and fall times are much smaller compared to propagation delay, then the output logic level (Z_1) changes after the propagation delay. In the above situation, oscillations will occur where the propagation delay determines the clock period of oscillations.

On the contrary, when the propagation delay is smaller than the rise or fall times, the output will start changing before the input has time to stabilize. This leads to a situation where a rising or falling input signal starts influencing itself in the opposite direction before it reaches the switching threshold. This behavior needs to be analyzed using dynamic analysis taking into account the transistor characteristics, node capacitances etc., as static analysis alone would not suffice.

The two cases are illustrated in D-BJT BiCMOS gates with a feedback bridging fault using SPICE simulation for an odd number of inverter chain (3 inverters) as shown in Figure 9. When the propagation delay was small, for example, one D-BJT BiCMOS gate, oscillations did not occur and the voltage level stabilized at an intermediate level (undefined). Effects of bridging resistance under feedback bridging conditions were studied. For low bridging resistances, the voltage level stabilized at intermediate level. However, as the value of bridging resistance was increased, the effect of bridging became insignificant, resulting in correct logic levels.

When propagation delay is sufficiently large (with 3 or more inversions of D-BJT BiCMOS stages),

Figure 10: Plots illustrating oscillations under bridging fault with feedback bridging (a) Input signal (b) Fault-free operation (c) Oscillations under feedback bridging.

oscillations occur. When the bridging resistance (R_X) is sufficiently small, the oscillations will touch either '0' or '1'. When propagation delay is just sufficiently large enough for oscillations, it will cause signals to cross the threshold voltage, and the requirement for oscillation [15] to occur is observed to be as given below

$$t_{pd} > \frac{t_r + t_f}{2}$$

Where t_{pd} is the propagation delay, t_r is the rise-time and t_f is the fall-time.

Example: SPICE simulation using a specific set of parameters for a chain of D-BJT BiCMOS NAND gates exhibited the following characteristics: t_{pd}/gate= 0.50 nSecs, t_r= 1.2 nSecs, t_f= 1.2 nSecs. The above characteristics suggest that oscillations would occur with a propagation delay of 1.5 nSecs for the device chain. Simulations do not exhibit oscillations with one device (t_{pd}=0.5nSecs) but oscillations do occur with a device chain of 3 (t_{pd}= 1.5 nSecs), as shown in Figure 10.

6 Conclusions

Effects of bridging faults in BiCMOS devices were examined. Range of resistance values affecting the logic levels in BiCMOS under bridging of logical nodes without feedback was presented along with their effects on noise immunity. Power supply current (I_{DDQ}) monitoring for detection of bridging faults was shown. Feedback bridging faults resulting in oscillations was presented.

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