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Gate Level Representation of ECL Circuits for Fault Modeling*

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Abstract

Bipolar Emitter Coupled Logic (ECL) devices can now be fabricated at high densities and lower power consumption. With the achievement of low power and high densities, ECL technology is expected to be used widely in high performance digital circuits. This necessitates the need for obtaining optimum gate level models for ECL circuits. A simple technique to obtain gate level model of an ECL circuit is presented. The gate level models obtained for 1-level and 2-level ECL using the transformation rules presented are the same as the fault models that provide higher coverage of physical failures.

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1 Introduction

Emitter Coupled Logic (ECL) devices using bipolar technology are generally used in applications where switching speed is more important than power dissipation and cost. Conventional bipolar ECL technology represents the state of the art in silicon speed, providing system propagation delays of the order of 300 to 500 pico seconds but the price paid for such speeds is very high power dissipation (1.5 mW or more per gate - way too much for VLSI densities) [1]. Recent advances in technology such as BIT1 [1] developed by Bipolar Integrated Technology have made it possible to fabricate bipolar ECL devices that take about 1/20 th the area of conventional ECL devices with speeds comparable to the fastest ECL, consuming only 1/10 th the power. With the achievement of low power, high speed, as well as high density, ECL technology is expected to be used widely in various high performance digital circuits. For example, Sparc architecture developed by Sun microsystems, is being implemented using BIT's new bipolar process [2]. The integrated ECL microprocessor chip contains 122,000 transistors. Even more highly integrated bipolar and bipolar/MOS chips are expected in future, further narrowing the gap between low cost workstations and high performance servers [2].

Transistor level shorts and opens many of the physical failures and defects in ICs [3]. Analysis of simple logic circuits suggest that transistor level testing provides a higher coverage of faults compared to that at gate level. In this paper, we first describe in Section 2 how we arrive at the gate level model and the transformation rules for obtaining the functional gate level model given the ECL circuit diagram. Functional gate level modeling applied to some complex ECL circuits are given in Section 3. Section 4 deals with fault modeling of ECL and conclusions are given in Section 5.

The issue of fault modeling of 1-level ECL gates has been addressed in [4] and that of 2-level ECL gates in [5], where augmented fault models were presented providing higher coverage of physical failures. Morandi et. al. [6], have proposed an ECL logic model obtained using a dictionary for translating each circuit element into a gate level description, which results in a complicated logic model even for simple ECL circuit descriptions.

The next section explains how we arrive at the gate level model and describe the transformation rules for obtaining the gate level model. The 2-input ECL OR/NOR basic gate

Figure 1: Circuit diagram of a 2-input ECL OR/NOR gate.

is shown in Figure 1, which is used as the basic building block in most implementations of current day ECL logic designs.

2 Gate Level Modeling of ECL

The 2-input ECL OR/NOR basic gate is shown in Figure 1 [7], which is used as the basic building block in most implementations of current day ECL logic designs. The temperature and voltage compensated bias network comprised of Q_4, D_1, D_2, R_6, R_7 and R_8 do not directly contribute to the realization of the output function. The network performs the function of providing stable reference to the differential amplifier.

In ECL circuits, the input circuit and differential amplifier configuration forms the most important part in the realization of the logic function and is shown separately in Figure 2. An equivalent gate level model of the same is shown in Figure 3a. The inverters U3 and U4 are obtained due to the resistors R_3 and R_4, which transform the currents driven by the transistors into equivalent voltage drops causing the behavior of inverter. The outputs of the differential amplifiers (x and y) are directly applied to the emitter follower (Q_5 and Q_6)

Figure 3: (a) & (b) Equivalent gate level model.

inputs as shown in Figure 1. Simplified gate level model shown in Figure 3b is obtained by combining the inverters U3 and U4 into the OR and NOR gates. An open on the source or drain terminals of nMOS/CMOS gates lead to the same output behavior. However, the output behavior of a bipolar ECL circuit [4, 5] is different under open collector and open emitter conditions (α and β of Figure 2). The emitter followers perform the function of buffer between input (base) and output (emitter) without any inversion which is equivalent to a non-inverting buffer. Addition of transistors in parallel to the input side of the differential amplifier would cause corresponding increase in the number of inputs to the OR and NOR gates. The gate level model of Figure 3a can be redrawn as shown in Figure 3b by combining the inverters U3 and U4 into the OR and NOR gates for obtaining a simplified gate level model.

A set of transformation rules have been devised as shown in Table 1, for translating a given ECL circuit into its equivalent gate level model. Using the set of transformation rules, ECL circuits

Based on the transformation procedure performed above for converting the circuit description of Figure 1 into gate level model of Figure 3b, a set of transformation rules can be formed as shown in Table 1.

The sub-circuit description and its equivalent gate level models as shown in Table 1 is described by following rules:

(a) The differential amplifier forms the basic circuit description for ECL logic. Configuring transistors in parallel results in an OR/NOR gate with corresponding increase in the number of inputs to the OR/NOR gate at the gate level model.

(b) When the input transistors and differential amplifiers are in series with corresponding reference voltages to each of the differential amplifiers, the resulting gate level model is an AND/NAND gate. This method of configuring transistors in series is known as series-gating.

(c) When the differential amplifiers are in series with the first level of input and differential amplifier transistors, the resulting gate level model is a decoder.

(d) Resistors performing the function of load resistors for differential amplifiers convert currents into voltages. In the gate level model, it is equivalent to inverters [6].

(e) Emitter followers perform the function of buffer between input and output resulting in non-inverting buffer [6].

Figure 4: Two-level implementation of $(A+B)(C+D)$ and $\overline{(A+B)(C+D)}$.

(f) Transistor outputs connected together is equivalent to an OR gate with corresponding number of inputs [6].

The transformation of ECL circuit description into final gate level model involves two steps. In the first step, the ECL circuit description is transformed into gate level model using the transformation rules. The second step involves in minimizing the gate level model using standard logic minimization procedures.

The gate level model obtained using the transformation rules is called functional gate level modeling as the ECL circuit description is being transformed into an equivalent gate level model which is functionally equivalent describing the function that the ECL circuit performs.

3 Gate level modeling of 2-level Complex ECL circuit

Having obtained the above rules for transforming the circuit level description into functional gate level model, we apply the rules to transform the 2-level complex ECL circuit description shown in Figure 4 to obtain the functional gate level model. The differential amplifier configurations formed by Q_1, Q_2, Q_3 for inputs A,B and Q_4, Q_5, Q_6 for inputs C,D are

Figure 5: (a) & (b) Equivalent gate level model for two-level implementation of $\overline{(A+B)(C+D)}$.

in series gating configuration. According to transformation rule (b), we get AND/NAND gates in the gate level model for the series gating configuration. Since the input transistors for A,B as well as C,D are in parallel, OR/OR gates are obtained in the gate level model according to transformation rule (a) with the set of OR/OR (for series gating ECL circuits) gate outputs connected to the inputs of the AND/NAND as shown in Figure 5a. Inverters are obtained for the resistors of the differential amplifiers at the output of the AND/NAND. Logic minimization is done in the next step by moving the inverters to obtain the final gate level model as shown Figure 5b. The minimized gate level models obtained for 1-level and 2-level ECL are the same as the fault models in [4, 5] that provide higher coverage of physical failures.

3.1 Functional Gate level modeling of ECL AND/NAND

Applying the rules to transform the ECL AND/NAND circuit description shown in Figure 6 to the obtain the functional gate level model. The series gating configuration formed by the transistors Q_2, Q_3, Q_4 and Q_5 is similar to rule (b). Transistor Q_1 forms the input transistor and hence acts as a buffer. Transistor Q_8 and Q_9 form emitter follower outputs resulting in buffers according to rule (e). Output resistors R_5 and R_6 result as inverters at the gate level. This results in the AND/NAND gate with output inverters as shown in Figure 7a. Logic

Figure 7: (a) & (b) Equivalent gate level model for two-level AND/NAND.

Figure 8: ECL series gating implementation of decoder.

minimization is done in the next step by moving the inverters to obtain the final gate level model as shown in Figure 7b.

3.2 Functional Gate level modeling of ECL Decoders

Applying the rules to transform the ECL decoder circuit description shown in Figure 8 to obtain the functional gate level model. The series gating configuration formed by the transistors to perform the decoding function is similar to the configuration shown in rule c. Hence, according to rule c, the ECL decoder circuit transforms to the gate level model shown in Figure 9. The resistors transform to inverters according to rule d. Logic minimization is done in the next step by moving the inverters to obtain the final gate level model as shown in Figure 10.

3.3 Functional Gate level modeling of D-type Flip-Flop

Applying the rules to transform the ECL D-type Flip-Flop circuit description shown in Figure 11 to obtain the functional gate level model. The series gating configuration formed by transistors Q_2, Q_4 and Q_5 results in gate G_1 and transistors Q_3, Q_6 and Q_7 results in gate

Figure 11: ECL implementation of an ECL D Flip-Flop.

Figure 12: (a) & (b) Equivalent gate level model of the ECL D Flip-Flop.

G_2 at the gate level shown in Figure 12a. Since transistor Q_5 and Q_6 outputs are connected together and is fed back as input to transistor Q_7, the feedback at the gate level connecting gate G_4 output to G_7 input is obtained. At the gate level, input inverters G_5, G_6 and G_7 are obtained according to rule c for ECL decoders. The final gate level model as shown in Figure 12b is obtained by moving the input inverters to the next level.

3.4 Functional Gate level modeling of D-type Flip-Flop with Q and $\overline{Q}$

Applying the rules to transform the ECL D-type Flip-Flop circuit description shown in Figure 13 to obtain the functional gate level model. The series gating configuration formed by transistors Q_1, Q_3 and Q_4 results in gates G_1 and G_2 at the gate level as shown in Figure 14a. Transistors Q_2, Q_5 and Q_6 results in gates G_3 and G_4 at the gate level. OR gates G_5 and G_6 are formed due to the collectors being tied together. Transistor Q_7 emitter being connected to the base of Q_5 forms the feedback path connecting output Q from gate G_8 output to input G_4. Similarly, gate G_7 output connection to G_3 input is due to the feedback formed by transistor Q_8 emitter to transistor Q_6 base. The final gate level model as shown in Figure 12b is obtained by moving the input inverters to the next level.

Figure 14: (a) & (b) Equivalent gate level model of the ECL D Flip-Flop with Q and $\overline{Q}$ outputs.

4 Fault Modeling of ECL OR/NOR

The issue of fault modeling of ECL OR/NOR gate is addressed separately [4, 5], however, the relevance of functional gate level model as an optimum fault model is addressed here.

For fault modeling of ECL circuits, classical stuck-at fault model was shown to be inadequate [4, 5] to represent most of the physical failures. An augmented stuck-at fault model was proposed, providing higher coverage of physical failures for 1-level [4, 5] and 2-level ECL circuits. The augmented stuck-at fault model proposed is the same as the functional gate level model obtained for 1-level and 2-level complex ECL circuit descriptions.

Thus, it is encouraging to note that the functional gate level models obtained for ECL OR/NOR and 2-level complex ECL circuit description using the procedure for transforming the circuit description into functional gate level models not only provide gate level models but the gate level models obtained are also fault models which provide full coverage (100 %) of all detectable physical failures of the circuit description. With the above results, it is expected that the functional gate level models obtained for the ECL circuit description also provide maximum coverage of all detectable physical failures of the ECL circuit description.

5 Conclusions

A set of transformation rules have been devised for translating a given ECL circuit description into its equivalent gate level model. The gate level model obtained using the transformation rules for 1-level and 2-level ECL gates are the fault models that provide higher coverage of physical failures.

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