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Modeling of Intra-Cell Defects in CMOS SRAM

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Abstract

The effect of defects within a single cell of a static random access memory (SRAM) is examined. All major types of faults, including bridging, transistor stuck-open and stuck-on, are examined. A significant fraction of all faults cause high IDDQ values to be observed. Faults leading to inter-cell coupling are identified.

1 Introduction

With the increase of cell density, not only does the probability of memory failures increase, but the nature of the failure modes becomes more complex and subtle [1, 2]. Many RAM test algorithms based on different fault models have been proposed. Activeness of test algorithms depends on the accuracy of the fault model, which is used to represent the physical failures [2, 3]. A widely used fault model for RAM devices was proposed by Nair et. al [4]. In this model, defects in the address decoder and the Read/Write logic are mapped onto functionally equivalent faults in the memory array. The advantage of this model is that all the faults can be considered to be stuck-at-0/1 in the memory array, with the addition of of state transition faults and data retention faults. Test algorithms for SRAMs, based on physical spot defects,

which are modeled as local disturbances in the layout of an SRAM cell and translated to defects in the corresponding transistor diagram, have been proposed.

In this paper, we examine fault models for the SRAM cell at the transistor level. We consider both functional and IDDQ monitoring. All major transistor faults are considered assuming hard shorts for the bridging faults.

2 Faults in Register Storage Elements

Recent studies have shown that the traditional stuck-at fault model is insufficient for modeling faults in storage elements. Reference [2] shows that a significant fraction of faults cannot be modeled as input/output stuck-at-0/1 for elementary register storage elements. Consider for example, the transmission-gate latch in Figure 1. Some faults cause the cell to exhibit *data-feed-through* behavior, i.e. the input data D or $\overline{D}$ is propagated to the output. Other faults cause the cell to exhibit *clock-feed-through*, i.e CLK or $\overline{CLK}$ is propagated to the output. These effects are discussed in [5] shows in detail. Besides the *feed-through* behaviors, some faults cause logic non-retention problems, always (NR) or conditionally (CNR). This means that cell works properly in the transparent phase, but not in the latching phase. Indeterminate faults are regarded to be parametric because they can be detected only by monitoring the quiescent supply current (IDDQ). Table 2 summerizes the faulty behavior of the cell in Figure 1.

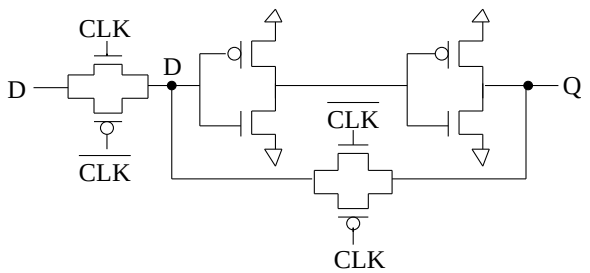

Figure 1: The transmission gate latch

Table 1: Behavior of the transmission-gate latch

Behavior	**% of testable faults**
stuck-at	45%
Feed-through	18%
NR/CNR	9%
Complex behavior	2%
Fault-free with delay	10%
Parametric	16%

3 Detailed Examination of the SRAM Cell

The static cells used in memory chips also use feedback to retain the latched signal. However a new logical value is forced in using a higher strength signal on the bit or $\overline{bit}$, rather than gating it in using a clock signal.

The common CMOS SRAM cell is shown in Figure 2. Two pMOS transistors are used as pull-up loads for the bit and $\overline{bit}$ lines. The pull-down transistors of the cross-coupled inverters are chosen to be two or three times wider than the pass transistor in order to avoid charge sharing during *read* operation. The two pull-up transistors of the inverters have minimum size to retain charge lost due to leakage current [6]. Although this cell is a storage element, the observations given in [3] for the fault analysis of the elementary storage elements cannot be applied for SRAM cells. This is because the SRAM is a symmetric structure with complimentary bidirectional inputs/outputs and the cell is only indirectly observable via the read circuitry. Here we consider all possible transistors stuck-on, stuck-open and bridging faults. Behavior of the cell under stuck-on/open faults is given in table 2. The results presented depend on the transistor sizing and the read circuitry. 'I' corresponds to IDDQ testable and 'i' corresponds to indeterminate behavior, which depends on the signal strength. Possible inter-cell coupling is indicated using the cx notation. For example 'cb' corresponds coupling involving the bit line. In the table, 'b', '$\overline{b}$', and 'w' correspond to bit, $\overline{bit}$, and word lines. The cell is said to be stuck-at, when the cell provides the same logic value when read.

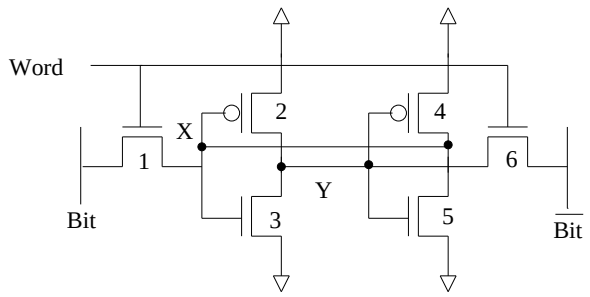

Figure 2: The SRAM cell

Table 2: Behavior of the SRAM cell under Stuck-on/open faults

Transistor	**Stuck-on**					**Stuck-open**		
	bit*	$\overline{bit}^*$				bit*	$\overline{bit}^*$	
1	–	–	NR1			H	L	SA1
2			fault-free					fault-free
3	H	L	SA1	I		L	H	SA0
4			fault-free					fault-free
5	L	H	SA0	I		H	L	SA1
6	–	–	NR0		$c\bar{b}$	L	H	SA0

Consider stuck-open fault in transistor 1. This fault isolates node X from the bit line. The *write* operation is not affected because of the signal received from $\overline{bit}$. During the *read* operation, the bit line is pulled-up, while the $\overline{bit}$ functions properly. This suggest that observing this fault depends on the read circuitry of the sense amplifier. If the design is such that the circuit responds to the variations in bit line faster than that of the $\overline{bit}$, then this fault appears as stuck-at-1. The sense apmlifier may cause high IDDQ when both bit and $\overline{bit}$ signal are 1. Similarly stuck-open fault in transistor 6 can be modeled as stuck-at-0. Stuck-on fault in transistor 1 connects the bit line with node X. The behavior of the fault is dependent on the logic value of node X and the relative strengths of the signals and is thus termed indeterminate. This fault can cause coupling between this cell and other cells through the bit line (cb). The same is true for the stuck-on fault in transistor 6. Stuck-open faults in transistors 2 and 4 cannot affect the functional behavior of the cell. Stuck-on faults in transistors 3 and 5, not only change the functional behavior, but cause increase in IDDQ due to the path between V_{dd} and V_{ss} when the fault is activated.

The behavior of the cell under all possible shorts is also examined. Results in Table 2 show that most faults change the functional behavior with increase in IDDQ during the *write* cycle. Some shorts causing the cell to be stuck-at may be dependent on the transistor dimensions. Shorts involving power nodes V_{dd} and V_{ss} With each X and Y nodes can enhance the IDDQ drawn by the cell.

Table 3: Behavior of the SRAM cell under possible intra-cell defects

1st. node	**2nd. node**	bit*	$\overline{bit}^*$	**Effect**		
V_{ss}	word	H	H	RD	I	word unaccessable
	bit	L	H	SA0	I	Bit line low
	$\overline{bit}$	H	L	SA1	I	$\overline{bit}$ line low
V_{dd}	word	–	–	NR0/1	I	word always accessed
	bit	H	L	SA1	I	Bit line high
	$\overline{bit}$	L	H	SA0	I	$\overline{bit}$ line high
word	bit	H	L	SA1	I	cbw
	$\overline{bit}$	L	H	SA0	I	c$\overline{b}$w
bit	$\overline{bit}$	–	–	RD	I	cb$\overline{b}$
X	V_{dd}	H	L	SA1		
	V_{ss}	L	H	SA0		
	Y	L	L	RD	I	
	word	H	H	RD	I	cw
	bit	–	–	NR1		cb
Y	V_{dd}	L	H	SA0		
	V_{ss}	H	L	SA1		
	word	H	H	RD	I	cw
	$\overline{bit}$	–	–	NR0		c$\overline{b}$

4 Conclusions

In this paper, we present a detailed examination of the SRAM cell. The results show that a large fraction of faults cause increase in IDDQ, which suggests that current testing can be very effective for SRAMs [7]. Some faults may not be detected without using IDDQ monitoring. The cost of testing can be reduced by designing the memory array for high current testability. The results presented here can be extracted by considering defects that affect multiple cells. Using inductive fault analysis, or using industrial data from actual

faulty chips, probabilities can be assigned to different failure modes. This can be used for optimization of test strategies.

Acknowledgment

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