A Bipartite, Differential I_{DDQ} Testable Static RAM Design

Waleed K. Al-Assadi
Anura P. Jayasumana
Yashwant K. Malaiya[†]

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Department of Electrical Engineering/
[†]Department of Computer Science
Colorado State University
Fort Collins, CO 80523

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W. K. Al-Assadi, A. P. Jayasumana, and Y. K. Malaiya†
Electrical Engineering Department
† Computer Science Department
Colorado State University
Fort Collins, CO 80523

Abstract

I_{DDQ} or current testing has emerged in the last few years as an effective technique for detecting certain classes of faults in high density IC's. In this paper a testable design that enhances the I_{DDQ} testability of static random access memories (SRAMs) for off-line testing is proposed. To achieve high accuracy and a test speed approaching the system operational speed, the memory is partitioned for comparison of I_{DDQ} values. Parallel write/read operations are used to activate possible faults, while quiescent power supply currents from two blocks are compared.

1 Introduction

Complexity of testing semiconductor memories has grown significantly along with the growing density of memory chips. As a result, the nature of the failure modes have become more complex and subtle. Testing large memories is a complex and expensive process. Several techniques have been developed to overcome the problem of large test time, such as built-in self test (BIST) and testable designs [1],[2],[3].

Existing test algorithms may not detect such chip defects as gate-oxide shorts, bridging defects, parasitic transistor leakage, defective p-n junction, transistors with incorrect threshold voltage, which cannot be mapped on to the classical stuck-at fault model. Some of these faults may not affect the logical behavior, but may affect the parametric or dynamic behavior. Chips with such defects may pass the functional tests but malfunction over time, causing reliability hazards [3]. Many of these faults cause elevated quiescent power

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supply current (I_{DDQ}). Defects such as shorts and abnormal leakage current cause a state-dependent elevated I_{DDQ}, which is typically several orders of magnitude greater than the I_{DDQ} of a fault-free device. An analysis of the effectiveness of I_{DDQ} testing has shown that I_{DDQ} testing is necessary to detect a significant fraction of the defects of a SRAM [3].

In SRAMs, most of the I_{DDQ} testable faults are activated during the write/read cycles [3],[4],[5],[6]. A write cycle forces most nodes to certain voltage levels, thus activating different faults. However, some faults may only be sensetized during the read cycle. Although writing to the cell is proper, the cell could flip its contents when electrically connected to the bit and $\overline{bit}$ lines. Such faults include coupling faults and neighborhood pattern sensitive faults. In the proposed scheme, I_{DDQ} testing is enhanced by allowing for parallel activation of words. This will allow many nodes to be activated simultaneously resulting in activation of I_{DDQ} testable faults [5].

In this paper, we propose a testable scheme for off-line testing that enhances the I_{DDQ} testability for CMOS SRAMs. The proposed scheme partitions the memory array into two identical partitions each with its own operational ground node. Quiescent power supply currents can be monitored during parallel access of locations or subset of locations (blocks) of each partition. Test speed is enhanced by comparing currents in the two partitions.

2 Testing SRAMS using I_{DDQ}

I_{DDQ} testing has been shown as an effective way in testing CMOS combinational circuits. I_{DDQ} testing can also be effective in detecting SRAMs defects that escape traditional voltage monitoring techniques. In [3], an analysis of the effectiveness of the I_{DDQ} testing has been done using SRAM of 8k X 8-bit words manufactured by philips, using Inductive Fault Analysis technique. The results show that a high fault coverage is achieved when I_{DDQ} testing is performed in combination with functional testing. In [7], experimental results were reported on deploying current testing to detect defects that cause data retention problems. A current-mirrored differential sense amplifier was used to compare the current response to that of a reference current. A word addressable 16K SRAM with built-in defects was considered. The results show I_{DDQ} testing is effective in detecting soft defects such as nMOS and pMOS floating gate faults. However, conventional voltage testing failed to detect all defective cells with a floating pMOS transistors.

The idea of I_{DDQ} testing is expanded for fault localization in [6]. In [8], a testable SRAM structure was proposed for observing the internal switching behavior of the memory cells. The proposed structure provides a very high coverage of disturb-type pattern sensitivity using a simple algorithm of complexity of 5n (n= number of memory cells). In [4], the detailed fault model of the 6-transistor memory cell was investigated for possible transistor level faults. It was shown that intra-cell defects can cause inter-cell faults in the memory

array, such as coupling faults. Such faults were shown to cause elevated I_{DDQ} when activated. In [5] a testable design for memory array was shown to enhance I_{DDQ} testing by allowing parallel access to the whole memory cells during the write cycle.

The above work clearly establishes the promise of I_{DDQ} testing for SRAMs. However, it does not establish testability requirements that can improve the effectiveness of current testing. In addition the above work does not address the problem of current measurements and the effects of the size of the circuit under test on the accuracy and testing speed.

3 Performance considerations of I_{DDQ} testing

The problems associated with the present I_{DDQ} testing techniques are the performance considerations of the built-in current sensors (BICS) that are being used to monitor the I_{DDQ}. Figure 1 shows the principle of I_{DDQ} monitoring. At the sampling edge, the virtual ground voltage V_G is compared with the reference voltage V_{ref}. The value of V_{ref} is carefully chosen such that $V_G < V_{ref}$ for fault free circuit and $V_G > V_{ref}$ for fault circuit with elevated quiescent current indicating a fault. A major problem with this scheme is its operational speed limitations. It is always preferred to perform test at operational system speed, but the presence of the BICS circuit significantly degrades operational speed. As the size of the circuit under test increases, the capacitance between the virtual ground and true ground increases and therefore large settling times are required for the I_{DDQ} to become stable resulting in a slow measurement process. To improve the performance of I_{DDQ} testing, circuit partitioning is performed in order to reduce the capacitance of the current sensing node (C in Figure 1) [9],[10]. The selection of the best reference value for the BICS circuit remains a problem. The proper selection for such value is essential for high reliability circuits. In addition, the partitioning problem for high density IC's to enhance the resolution of I_{DDQ} testing, also need to be addressed in details. This paper attempts to address some of the above problems.

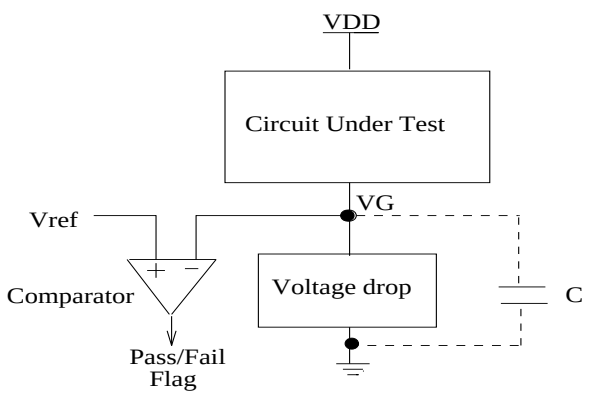

Figure 1: Principle of I_{DDQ} testing

4 I_{DDQ} Testable SRAM Principle

A new testable scheme for SRAMs that enhances I_{DDQ} testing for off-line testing is proposed. This scheme is intended to minimize the impact of the conventional built-in current sensor (BICS) circuit on circuit's performance by achieving test speed approaching the system operational speed. The memory array is partitioned physically into two identical partitions each with its own operational ground node. The operational ground nodes are used during normal operations, thus bypassing the current comparator. During the test mode, the two operational ground nodes are open, and the test ground node (ground node of the current comparator) will be the common ground node for the circuit. This can be done by the tester. Identical partition sizes implies allows equal ground line capacitance for each partition. A built-in current comparator (BICC) is used to compare the quiescent power supply currents of the two partitions during the testing mode while accessing their locations simultaneously. If the difference between the two currents (|I1-I2|) (in Figure 2) exceeds a pre-designed threshold value I_{th}, a flag raises indicating a fault in one of the partitions. If the difference is less than I_{th}, then it either indicates a fault free case or indicates an identical fault in both partitions. The faulty to fault free current ration of a cell indicates how many cells can be activated in parallel and still detects the fault. To overcome this problem, each partition can be divided into blocks. A block is a subset of contiguous or interleaved memory locations. Testing can be employed by simultaneously accessing two identical blocks, each belonging to a separate partition. Reducing the size of the accessed array will allow the resolution to be maintained. In addition, reducing the size of the partition maintains the number of parrallely activated cells at a reasonable number, and this will ensure that leakage currents will not add up to the point where they become comparable to the abnormal quiescent current expected of a fault. Therefore the accuracy and testing speed expected to be improved significantly.

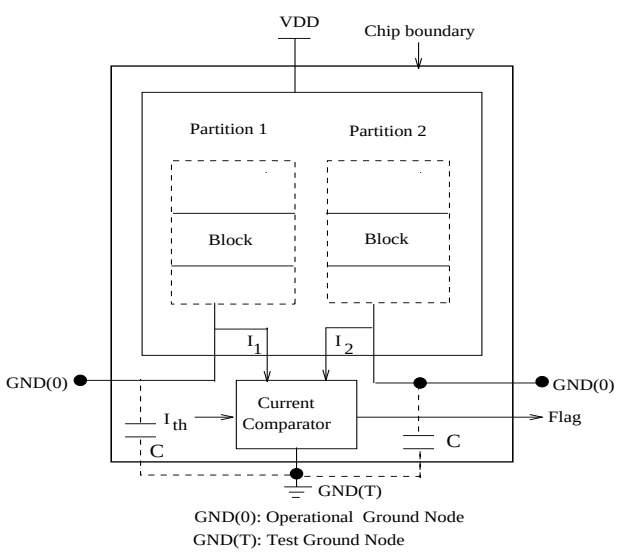

Figure 2: Principle of I_{DDQ} comparison

5 I_{DDQ} Testable SRAM Design Considerations

In this section we consider the proposed I_{DDQ} testable SRAM design. The basic objective is to achieve a I_{DDQ} testable scheme with high test accuracy and speed with small hardware overhead. We assume that the memory system is a word oriented architecture. Design modifications are aimed at achieving three basic goals:

1 Efficient partitioning of memory array into identical blocks of a reasonable size.

2 Block write/read operations during the testing mode to access locations within a block in each partition in parallel.

3 Efficient BICC circuit with high sensitivity and accurate I_{th} selection.

To achieve the first and second goals, modifications to the peripheral circuits are required. In order to clarify the design modifications, consider the a memory array of 8K x 8-bit words. This circuit can be physically partitioned into two identical arrays each of 4K X 8-bit words. Each word line drives two memory locations, each in one partition. The address register size is 13 bits. A test signal (t) is used such that during normal operation mode t=0, and only one partition is selected for normal word access. a_0 selects the partition. The remaining 12 bits are used to decode 1-out of-4K locations of each partition. The write operation is performed when $\overline{W}/R$ signal is zero. The bit drivers consists of tri-state inverters controlled by the partition select logic. This logic constitutes the least significant bit (a_0) of the address register, the test signal (t) and the $\overline{W}/R$ signal as shown in Figure 3. During the test mode t=1 and both partitions are accessed simulatenously for parallel write/read operations.

The most crucial issue is the address decoder modifications that allow selective access to several word locations, either physically contiguous or physically interleaved simultaneously. The conventional address decoder is modified to allow two modes of operation, normal and testing. To achieve high test speed, the process of current comparisons is needed to be limited to a minimum number, which implies minimum number of comparand blocks needed (goal 1 above). For the example under consideration, we assume that each 4K X 8-bit words can only be divided into four blocks. In general it can be more than four blocks depending on the size of the memory array.

During the normal operation mode (t=0), the decoder works normally and is able to activate only one word line for each write or read operation. During the testing mode (t=1), the decoder is able to activate one block of locations simulatenously. To achieve this mode of operation, the two lower bits a_1 and a_2 of the address register, and the test signal (t) are used to perform block selection during the testing mode as shown in Figure 3. In the test mode, each partition contains four blocks. Physical locations of the four blocks are interleaved with each other. The remaining higher order bits are to select the locations

within the block in the normal mode of operation. The operation is such that during the testing mode, the AND gate that corresponds to a combination of (a_2, a_1) is active , thus the corresponding 1K address lines of the address decoder are active. These active lines of the address decoder are going to select 1K interleaved words as (a block) in each partition. These two blocks are accessed simulatenously. The currents from both blocks are compared while parallel write/read operations are performed into both blocks. From this design shown in Figure 3, only one block is selected from each partition for current comaparision.

6 Testing Modes

Faults that enhance I_{DDQ} are mainly transition faults, state coupling and bridging faults, and neighborhood pattern sensitive faults. To detect state coupling and bridging faults in a word-oriented architecture, all states of two adjacent cells i and j in a word should be considered [11]. The testing sequence contains a set of parallel write/read operations to the blocks, such that if a test vector v is applied to *block* i, then $\overline{v}$ is applied to *block* $(i+1)$. The proposed test sequence contains two test vectors with their complements; they are (00000000), (11111111), (01010101) and (10101010). This test sequence is capable of detecting all possible state coupling and bridging faults, and transition faults. For each test vector applied, four block write/read operations are required as shown:

Write: block 0 $\leftarrow$ (00000000)
Write: block 1 $\leftarrow$ (11111111)
Write: block 2 $\leftarrow$ (00000000)
Write: block 3 $\leftarrow$ (11111111)
Read : block 0
Read : block 1
Read : block 2
Read : block 3

Although neighborhood pattern sensitive faults are considered complex faults require a series of write/read operations into small sets of interleaved locations, the sequence above is capable of detecting some of those faults. From above, it is clear that 16 parallel write/read operations are required to test the SRAM for the faults assumed. This scheme may not cover some non I_{DDQ} testable failure modes which may need to be considered separately.

The known SRAM testing algorithms have a complexity proportional to n, where n is the number of memory locations. With the testable scheme proposed, the complexity of testing is proportional to b, where b is the number of blocks. Since $b \ll n$, the testing

process is speeded-up by a factor of b/n. However the accuracy of testing depends also on the performance and sensitivity of the comparator BICS used for current monitoring. It should be noted that the differential BICS reported in [9] can be used in this scheme. With this BICS circuit, for each write/read operations, testing is performed in two phases instead of one phase as suggested in this paper.

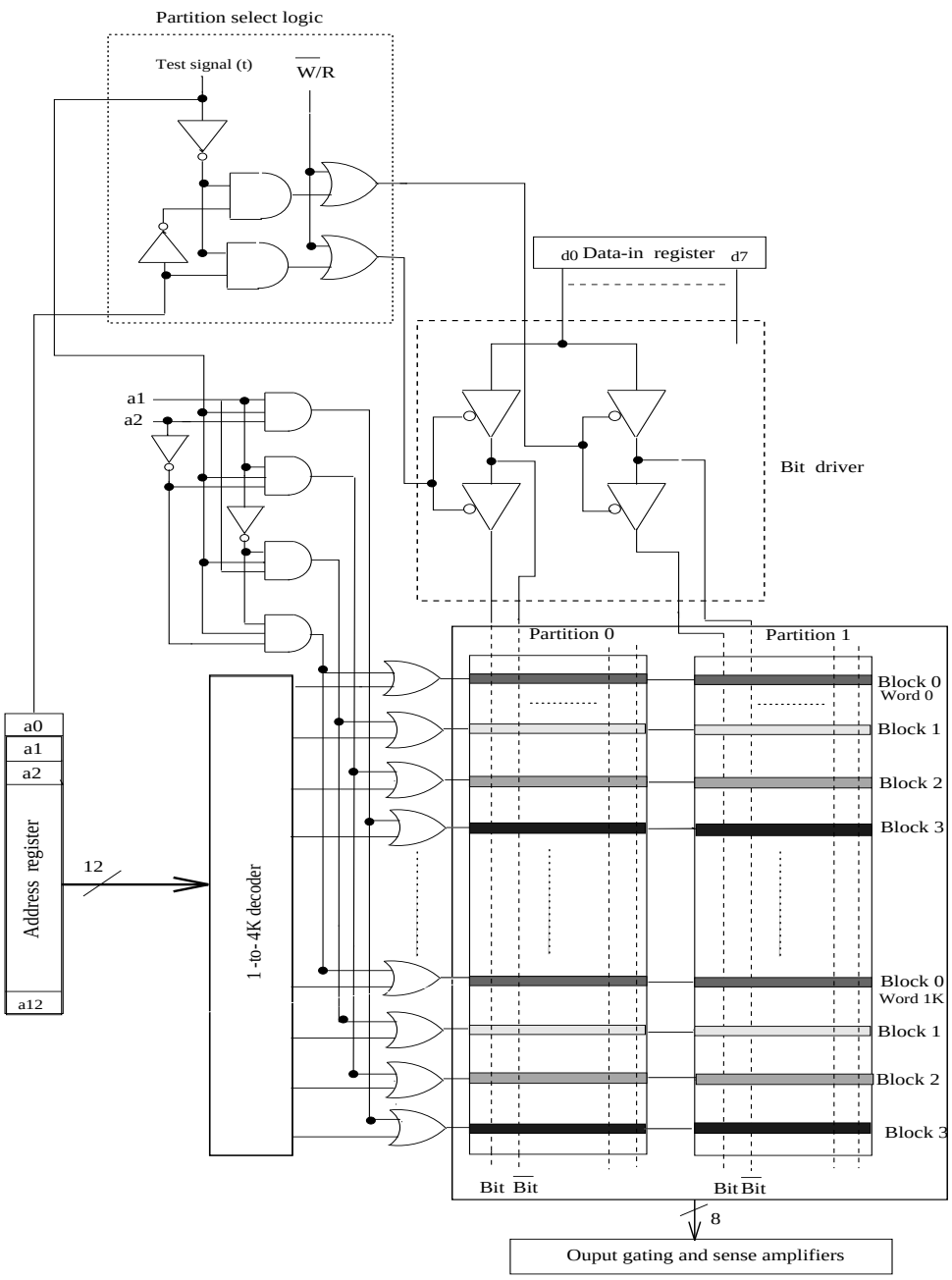

Figure 3: The I_{DDQ} 8K X 8 testable SRAM

7 Conclusions

This paper presented a scheme for I_{DDQ} testable SRAM. The proposed scheme employs memory array partitioning and parallel write/read operations, during which several faults are activated with elevated quiescent power supply current. The currents are compared in one phase for each opearion. This, we think, enhances the testability such that testing can be performed in speeds approaching the system operational speed. However, several questions remain unanswered in this area. For example, how to make optimal partitioning such that it will not add more hardware overhead, and accordingly how to make the selection of the of the threshold current I_{th}.

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