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PROFESSIONAL PREPARATION

University of Delft, Holland	Mathematics and Computer Science	BSc	1972
University of Delft, Holland	Mathematics and Computer Science	MSc	1974
University of Utrecht, Holland	Computer Science	PhD	1984

APPOINTMENTS

1974-1978	Researcher	Mathematical Center, Amsterdam, Holland
1978 - 1984	Lecturer and Research Assistant	University of Utrecht, Holland
1984 - 1989	Lecturer and Research Fellow	University of Manchester, United Kingdom
1990 - 1996	Associate Professor	Colorado State University
1996 - present	Professor	Colorado State University

TEACHING AWARDS

2005 CSU College of Natural Science Excellence in Undergraduate Teaching Award
2007 CSU Eddy (Liberal Arts and Natural Sciences) Teacher Award

RELEVANT RESEARCH PUBLICATIONS

- B. Draper, R. Beveridge, W. Böhm, C. Ross, and M. Chawathe. Accelerated Image Processing on FPGAs, *IEEE Transactions on Image Processing*, Vol. 12, December 2003.
- G. Venkataramani, W. Najjar, F. Kurdahi, N. Bagherzadeh, W. Böhm and J. Hammes. Automatic Compilation to a Coarse-grained Reconfigurable System-on-Chip. *ACM Transactions on Embedded Computing Systems*, 2003.
- W. Böhm, J. Hammes, B. Draper, M. Chawathe, C. Ross, R. Rinker, and W. Najjar. Mapping a Single Assignment Programming Language to Reconfigurable Systems *Supercomputing*, 21:117-130, 2002.
- R. Rinker, M. Carter, A. Patel, M. Chawathe, C. Ross, J. Hammes, W. Najjar, W. Böhm, An Automated Process for Compiling Dataflow Graphs into Reconfigurable Hardware, *IEEE Transactions on VLSI Systems*, Vol 9, No 1, pp. 130-139, 2001.
- W. Böhm, B. Draper, W. Najjar, J. Hammes, R. Rinker, M. Chawathe, C. Ross, *One-step Compilation of Image Processing Applications to FPGAs*, *IEEE Symposium on Field-Programmable Custom Computing Machines*, May, 2001.

SIGNIFICANT RESEARCH PUBLICATIONS

- A.P.W. Böhm, *The Power of Streams*, Invited presentation, Reconfigurable Systems Summer Institute, National Center for Supercomputing Applications, UIUC Urbana Champaign, July 2006.
- Charlie Ross and Wim Böhm, *A Co-Verification Tool for a High Level Language Compiler for FPGAs*, *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM06)*, 2006.
- A.P.W. Böhm, J. Hammes, S. Sur, On the performance of pure and impure parallel functional programs, *Parallel Computing Journal*, Vol. 25, no 13-14, pp 1723-1740, 1999.
- J. Hammes, O. Lubeck, and A.P.W. Böhm, Comparing Id and Haskell in a Monte Carlo Photon Transport Code, *Journal of Functional Programming*, Vol. 5, Part 3, pp 283-316, 1995.
- S. Sur, A.P.W. Böhm, *Analysis of Non-Strict Functional Implementations of the Dongarra-Sorensen Eigensolver*, *Proc. International Conference on Supercomputing 1994*, pp 412-418, Manchester, UK, 1994.

RECENT FUNDING

S. V. Rajopadhye, A.P.W. Böhm *High Level Programming of High Performance Embedded Computing Systems*, National Science Foundation, *Bringing Research Results into the Undergraduate Curriculum* program, Contract Id: 0306124, \$ 629,926, 2003-2005, extended to 2007.

W.A. Najjar, A.P.W. Böhm, J.R. Beveridge, B. Draper (CSU); A.C Moorman, P.Humphrey, D.M. Cates (KRI) *Optimized Compilation of Visual Programs for Image Processing on Adaptive Computing Systems*, ARPA Contract, total cost to the agency: \$ 1,727,359, 1998 - 2001.

SYNERGISTIC ACTIVITIES

Teaching: Created first year Robot Programming and Games Programming Challenge Classes. Redesigned the two first year Computer Science courses to integrate theory and practice. Organized the CSU ISTeC High School Robot Programming Competition, 2006 and 2007.

Software Projects: *SA-C on Reconfigurable Systems*. A large body of software, spanning more than 250,000 lines of code, written by eight graduate students, consisting of compilers, simulators and viewers.

Functional Numerical Kernels and Applications. Kernels such as FFTs, and Eigensolvers, and complete applications, such as Monte Carlo Particle Transport Codes, were written in a variety of functional programming languages (Id, Haskell, Sisal) to assess their efficiency and expressiveness.

Reviewing: Member of program committees for PACT (Parallel Architectures and Compiler Technology), MPPM (Massively Parallel Programming Models), and Micro, for multiple years. Reviewer for the Journal of Parallel and Distributed Computing, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Software Engineering, Journal of Systems and Software, The Computer Journal, The Journal of Parallel Computing. University of Monash MSc and PhD reviewer.

COLLABORATORS & OTHER AFFILIATIONS

Recent Collaborators: W. A. Najjar, University of California Riverside, Arvind, Massachusetts Institute of Technology, J. L. Gaudiot, University of Southern California, J. Feo, University of California San Diego, R. R. Oldehoeft, Los Alamos National Laboratory, R. Hiromoto, University of Idaho, P. James Roxby, Xilinx Inc., J. Hammes, S.R.C. Inc.

Graduate Advisor: J. van Leeuwen, University of Utrecht, Holland.

SELECTED GRADUATE ADVISEES:

Masters: *A VHDL Run Time System for Dataflow Execution on Reconfigurable Systems*, 2000, Charlie Ross. *A dataflow graph to VHDL Compiler*, 2000, Monica Chawathe. *SA-C to VHDL Compiler Testing*, 2001, Aparna Shivaswami. *Design and Software Implementation of the SA-C Abstract Hardware Architecture*, 2001, Pankaj Patil. *Scheduling Fixed Point FFT Blocks on FPGAs*, 2001, Pramod Cherukumilli. *Encryption Algorithms in SA-C*, Madhusudan Kovalmudi, 2003. *A MacroProcessor for the LC-2*, Hari Aiyer, 2004. *Cordic Algorithms in SA-C*, Rama Chitta, 2004. *Horizontal Loop Unrolling in the SA-C Compiler*, Sumanth Kakaraparthi, 2004. *Integration of Reduction Operators in a Compiler for FPGAs*, Manju Matha, 2007.

PhD: *Distributed Runtime Support for Task and Data Management*, 1993, Matt Haines. *The Spectrum of Thread Implementations*, 1995, Bhanu Shankar. *Data Dependence Analysis for Functional Array Construction*, 1995, David Garza. *Expressiveness and Efficiency of Declarative Programming Languages*, 1995, Sumit Sur. *Compiling SA-C (Single Assignment C) to Reconfigurable Computing Systems*, 2000, Jeff Hammes. *Hardware Compilation of Streams and Processes*, 2006, Monica Chawathe. *An Abstract Target Architecture for FPGA Compilation*, 2006, Charlie Ross.