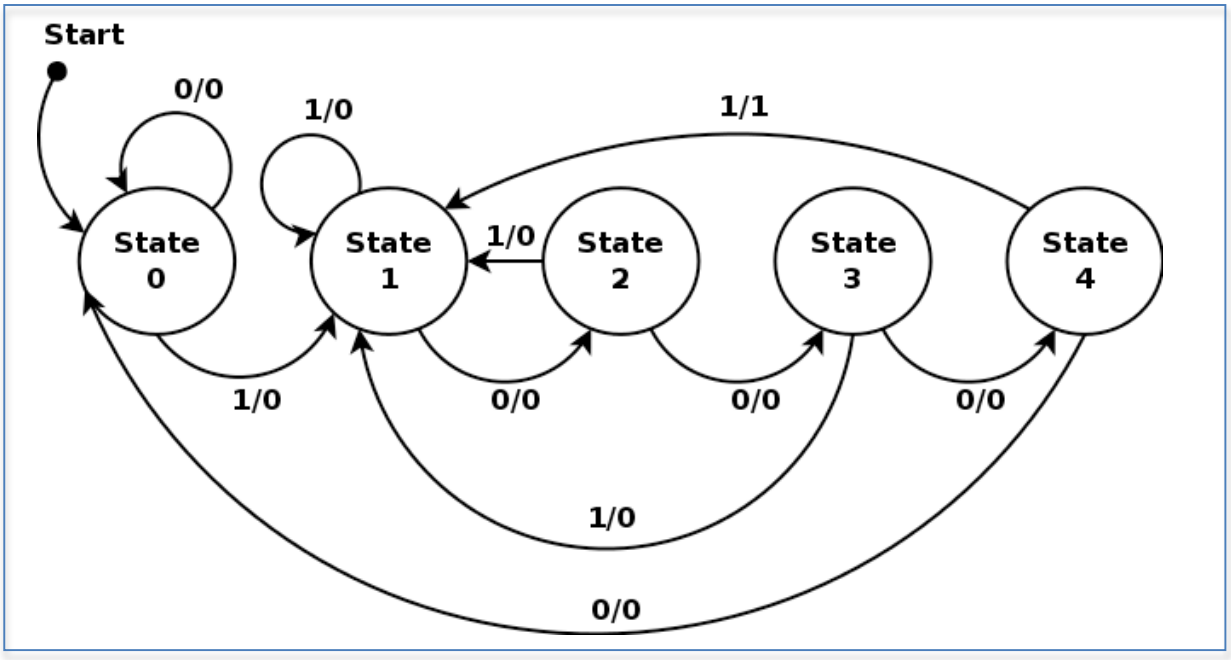
CS270 Homework Assignment 3 (HW3)

Due Sunday, October 12 at 10pm, no late submissions.
Homework and programming assignments are to be done individually.

Instructions: Design a Logisim circuit that implements the state machine shown below:



Here are a few clarifications that may help you, and questions you should be able to answer:

- What is the sequence of bits that is detected by this state machine?
- State should be stored in D-latches, how many do you need?
- The truth table is combinational logic similar to what you have already done.
- You must use a D-latch the output, since it's on a transition.
- Optimization is allowed and encouraged, the fewer gates the better!
- Why are there only 10 rows in the truth table instead of $2^4 = 16$?

Current State	*Input*	*Output*	*Next State*
000	*0*	*0*	*000*
000	*1*	*0*	*001*
001	*0*		
001	*1*		
010	*0*		
010	*1*		
011	*0*		
011	*1*		
100	*0*		
100	*1*		

Create a Logisim circuit called HW3 and turn it in to the RamCT drop box. You will be asked about your circuit at your recitation during the week of October 13.