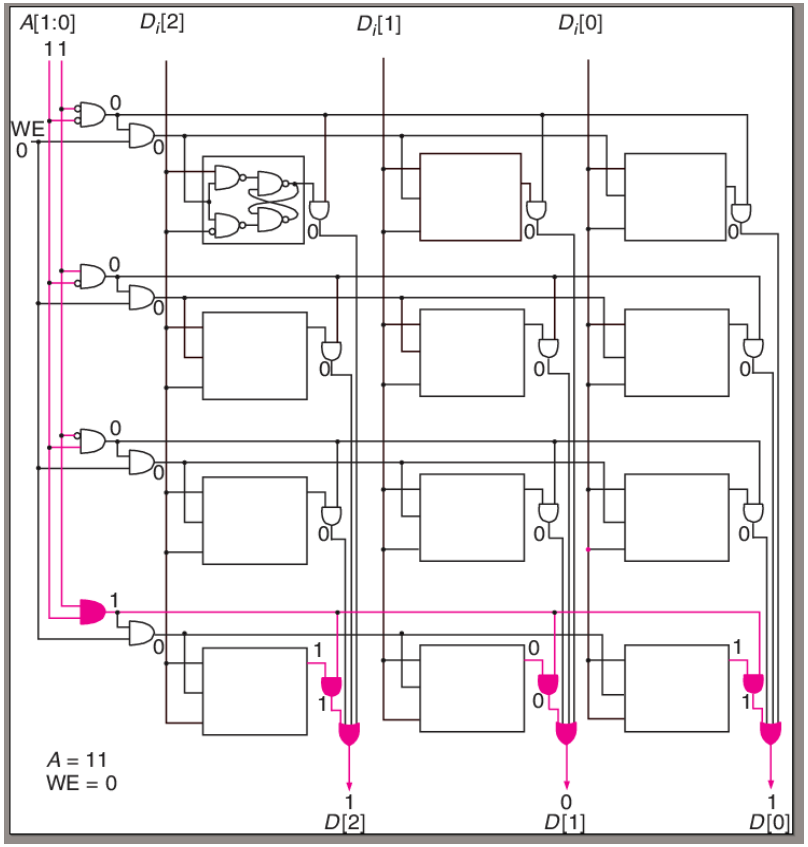
Peer Instruction #5: Memory and LC-3 Architecture

What is the address space and addressability of the memory shown, and what is the circuit doing?



A. 2^2, 3-bits, writing 00

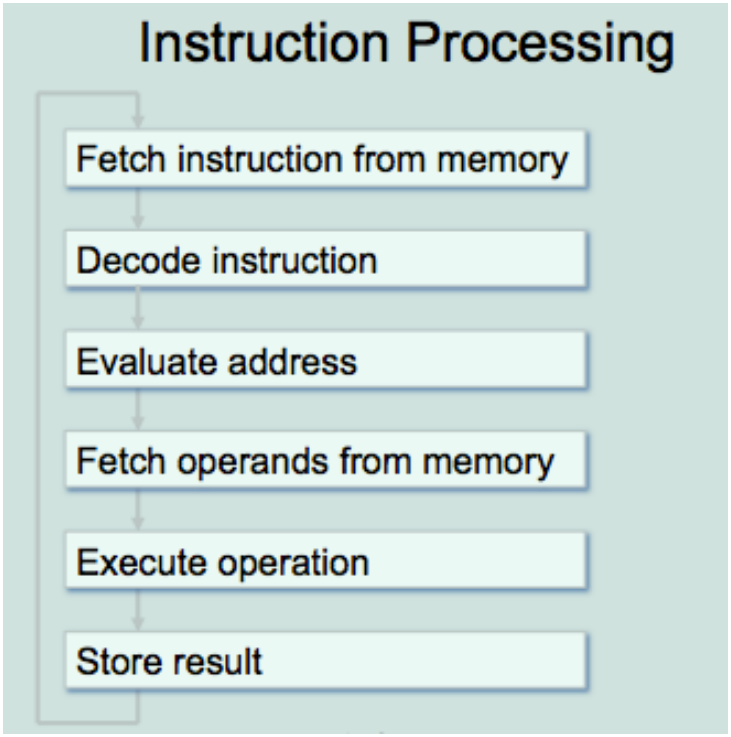
B. 2^3, 4-bits, writing 11

C. 2^3, 4-bits, reading 00

D. 2^2, 3-bits, reading 11

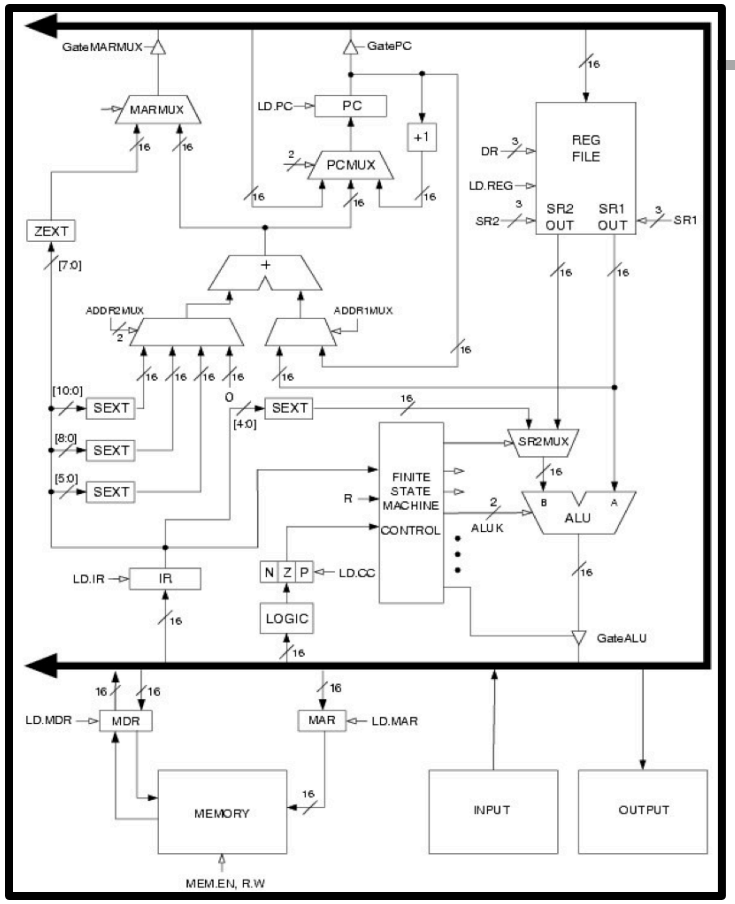
E. None of the above

Which instructions require the "Evaluate Address" cycle during instruction processing on the LC-3?



A. Load (LD)
B. Store (ST)
C. Branch (BR)
D. Jump (JMP)
E. All of the above

Which registers store the instruction currently being decoded and the address of the next instruction?



A. IR, PC
B. MDR, MAR
C. SR1, SR2, DR
D. MDR, PC
E. None of the above

What is the address space (number of locations), addressability (number of bits), and number of registers on the LC-3.

A. 2^{16}, 8, 8
B. 2^{16}, 16, 16
C. 2^{16}, 32, 16
D. 2^{32}, 32, 16
E. None of the above

LC-3 Architecture

What does the assembly instruction ADD R1,R2,R1 do?

A. Read R1, add it to R1, store in R2
B. Read R2, add it to R1, store in R2
C. Read R1 and R2, add them, store in R2
D. Read R1 and R2, add them, store in R1
E. None of the above

LC-3 Instruction

What does the assembly instruction 0x3206?

A. LD – load from memory
B. RET – return from subroutine
C. JSR – jump to subroutine
D. ST – store to memory
E. None of the above

LC-3 Instruction