

CS270 Recitation 15

“Final Exam Review Session”

Goals

To help students study some of the material from early in the semester to prepare for the final exam:

1. Numerical Representation: number conversion and floating-point addition
2. Simple Circuits: transistor circuits, combinational logic, and sequential logic

Due to limitations on time and resource, we will not cover LC-3 architecture or assembly coding, or C programming.

Sample Questions

NUMERICAL REPRESENTATION

1) What is the binary equivalent of the hexadecimal number 0xF0A9?

0b_____

2) What is the hexadecimal equivalent of the binary number 0b1101011110100001?

0x_____

3) What is the decimal equivalent of the binary number 0b11001010?

4) What is the binary equivalent of the decimal number 292?

0b_____

5) Translate the decimal values below into 8-bit 2's complement binary values and do the arithmetic.

12		15
	+	
+ 7		-4
	=	
= 19		= 11

0b_____ 0b_____

0b_____ 0b_____

0b_____ 0b_____

HINT: Assume IEEE 754 single-precision format for problems 6-7, which has 1 sign bit, 8 exponent bits, biased by 127, and 23 fractional bits, with an implicit 1.

6) What are the **binary** values of the fields of the IEEE 754 single-precision format of 3.125?

Sign = _____

Exponent: _____

Mantissa: 1. _____

7) What is the **decimal** number represented by 0b 1 1000011 10100000000000000000000?

8) Fill in the values below to add the single-precision floating point numbers $x = 2.25$ and $y = 4.50$.

$x = 2.25 = 0x40100000$, $y = 4.50 = 0x40900000$, $sum = x + y$

What is the (unbiased) exponent of x, in decimal? _____

What is the (unbiased) exponent of y, in decimal? _____

What is the mantissa of x in binary, with the implicit 1 shown? 1. _____

What is the mantissa of y in binary, with the implicit 1 shown? 1. _____

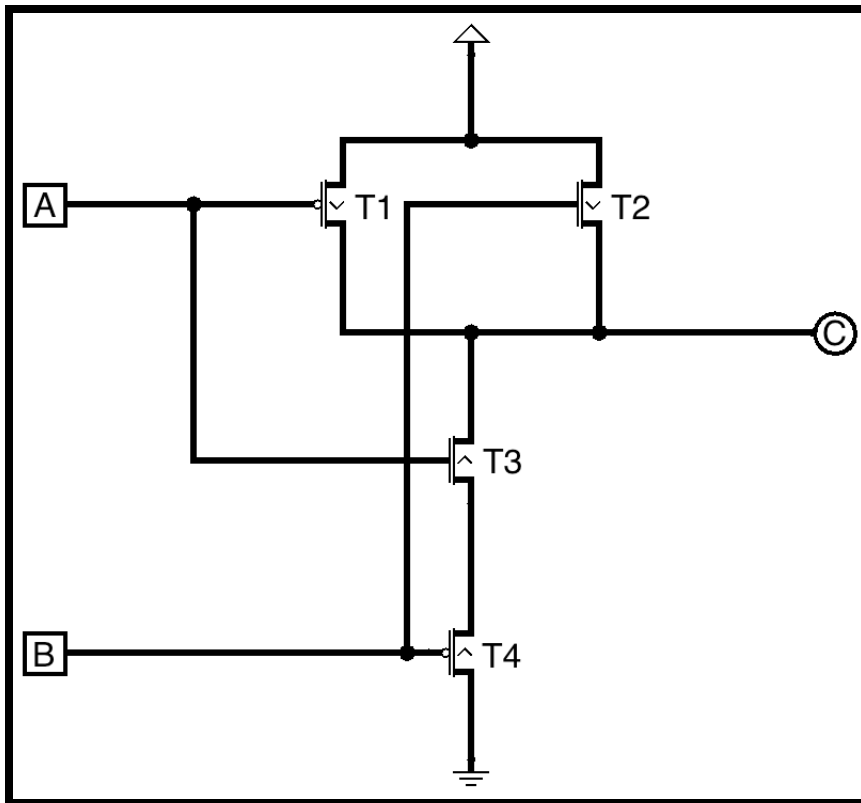
What is the mantissa of the sum after normalization? 1. _____

What is the (unbiased) exponent of the sum, after normalization? _____

What is the hexadecimal value of the sum? 0x _____

What is the decimal value of the sum? _____

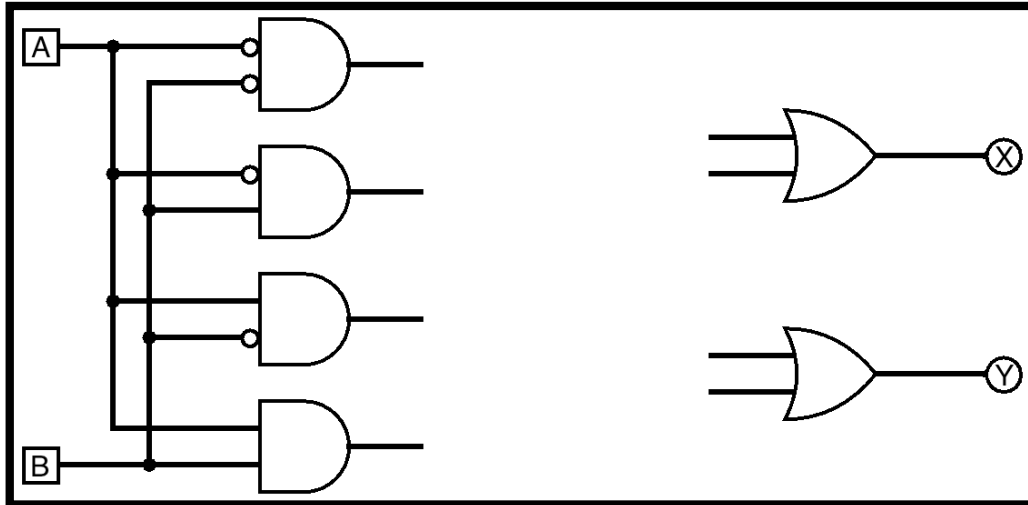
9) Analyze the transistor circuits shown below and complete the truth table.



A	B	T1 (p-type)	T2 (n-type)	T3 (n-type)	T4 (p-type)	C
0	0	Closed		Open	Closed	1
0	1			Open	Open	
1	0		Open			
1	1	Open	Closed	Closed	Open	1

10) Connect the output of the appropriate AND gates to the OR gates to fulfill the truth table below.

A	B	X	Y
0	0	1	0
0	1	0	1
1	0	0	0
1	1	1	1



11) Fill in the truth table for the D latch circuit show below.

Data (D)	Enable (EN)	Previous State	Output (Q)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

