CS370 Operating Systems
Colorado State University
Yashwant K Malaiya
Fall 2017

Slides based on
• Text by Silberschatz, Galvin, Gagne
• Various sources
What do these terms mean?

- Operating Systems
- Virtual
- Concurrent
Topics covered in this lecture

- Course Overview
- Expectations
- Introduction
Course webpage

- All course materials will be on
  - the course webpage
    - http://www.cs.colostate.edu/~cs370
  - canvas

- Schedule
- Lectures
- Assignments
- Announcements
- Grades will be posted on Canvas
- The course website and canvas are live now
Contacting us

• Instructor
  
  **Yashwant Malaiya**
  Computer Science (CSB 364)
  Office Hours: 11-12 Monday, 2:30-3:30 PM Thursday

• GTAs
  
  **Rejina Basnet, Nikhila Chireddy**
  Office Hours in CSB 120: TBA, TBA

• UTAs: **Phil Sharp, Kira Miller**

• All e-mail should be sent to cs370@cs.colostate.edu
• The subject should start as **CS370: ...**
Topics we will cover in CS 370

• Processes and Threads
• CPU Scheduling
• Process Synchronization and Deadlocks
• Memory Management
• File System interface and management
• Storage Management
• Virtualization
Textbook

• Operating Systems Concepts, 9th edition
  Avi Silberschatz, Peter Galvin, and Greg Gagne
  Publisher - John Wiley & Sons, Inc.
  (The Dinosaur Book)

• May also use materials from other sources including
  – Andrew S Tanenbaum, Modern Operating Systems
  – Thomas Anderson and Michael Dahlin, Operating Systems Principles & Practice
  – S. Pallikara, R. Wakefield
  – Other sources
On the schedule page

• Topics that will be covered and the order in they will be covered
• Readings - chapters that I will cover
• May also see chapters mentions of other resources besides the textbook
• Schedule for when the assignments will be posted and when they are due
  – Subject to dynamic adjustment
Grading breakdown

• Assignments: 30%
  – Programming & written
• Quizzes 10%
  – On-line, in-class
• Mid Term: 20%
• Project: 15%
• Final exam: 25%
Grading Policy I

• Letter grades will be based on the following standard breakpoints:
  
  >= 90 is an A, >= 88 is an A-, 
  >=86 is a B+, >=80 is a B, >=78 is a B-, 
  >=76 is a C+, >=70 is a C, 
  >=60 is a D, and <60 is an F. 

• I will not cut higher than this, but I may cut lower.

• There will be no make-up exams
  
  – Except for documented
    
    • required university event
    
    • acceptable family or medical emergency
Grading Policy II

• Plan: Every assignment will be posted about 2 weeks before the due date.
  – Every assignment will include information about how much it will count towards the course grade, and how it will be graded.

• Late submission penalty: 10%/day for the first 2 days and a ZERO thereafter.

• Detailed submission instructions posted on course website.

• Plan: Assignments will be graded within 2 weeks of submission
What will Quizzes and Tests include?

• I will only questions about what I teach or ask you to study
  – If I didn’t teach it, I won’t ask from that portion
  – Some on-line quiz questions about current state of technology may require you to search for an answer on the web

• If the concepts were covered in my lectures/slides/assignments
  – You should be able to answer the questions

• I will try to avoid questions about arcane aspects of some esoteric device controller
Exams

- One mid-term (20%)
- The final exam is comprehensive, but more emphasis on the later part (25%)
- There will be 10-12 quizzes (in class or online) (10%)
  - we may convert some homework into on-line quizzes
- Programming/written assignments
  - 30% of your course grade
- If you walk into class more than 20 minutes late, there is an automatic 75% deduction on the quiz score.
Term Project

• Group based
  – Logistics to be determined

• Options:
  – term paper on current/developing technology
    • Paper, presentation, poster?
  – Embedded system development

• The term project is a group assignment
  – More details later

• Tentative topics (to be determined later)
  – Multi-core Architectures
  – Reliability/Security
  – ?
Electronic devices in lecture room

• Permitted only in the last row, with the pledge that you will
  – not distract others
  – use it only for class related use
  – turn off wireless
Be kind to everyone

- You will be courteous to fellow students, instructor and teaching assistants
  - Classroom, outside, discussion board
- Do not distract your peers
  - No chatting
  - No eating
  - No cellphone use
Help me help you

• Surveys at the end of a class
• You will provide a list of
  – 2 concepts you followed clearly
  – 2 concepts you had problems keeping up
• Questions of interest for the majority of the class will be addressed in the next class
Help Sessions

• To be scheduled soon
• TAs will discuss a few key skills
  – Participation encouraged
  – Slides and videos will be on the web site
• Soon
  – C, pointers, dynamic memory allocation
  – Needed for upcoming programming assignment
ABOUT ME

Research

• Computer security
  – Vulnerability discovery
  – Risk evaluation
  – Impact of security breaches
  – Vulnerability markets

• Hardware and software
  – Testing & test effectiveness
  – Reliability and fault tolerance

• Results have been used by industry, researchers and educators
About me

• Teaching
  – Computer Organization (CS270)
  – Operating systems (CS370)
  – Computer Architecture (CS470)
  – Fault tolerant computing (CS530)

• Professional
  – Organized international conferences on Microarchitecture, VLSI Design, Testing, Software Reliability
  – Computer Science Accreditation: national & international
  – Professional lectures
EXPECTATIONS

• You are expected to attend all classes
• Assignments have to be done individually
• Expect to work at least 6-8 hours per week outside of class
  – Coding and reviewing material from class
• If you miss a lecture?
  – Add about 3 hours per missed lecture
Expert view on How to fail this class?

• Believing that you can learn via osmosis
• Missing lectures
  – “If you don’t have the discipline to show up, you will most likely not have the discipline to catch up”
  – Procrastinating
  – Get started on the assignments early
Interactions

• You can have discussions with me, the GTA, UTAs, and your peers

• But note
  – No code can be exchanged under any circumstances
  – No one takes over someone else’s keyboard
  – No code may be copied and pasted from anywhere, unless provided by us

• Bumps are to be expected along the way
  – But you should get over this yourself
  – It will help you with the next problem you encounter
Operator ...

Switchboard Operator

© UCB

Computer Operators
Gordon Moore (co-founder of Intel) predicted in 1965 that the transistor density of semiconductor chips would double roughly every 18 months.

2X transistors/Chip Every 1.5 years
Called “Moore’s Law”

Microprocessors have become smaller, denser, and more powerful.
## Computer Performance Over Time

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Uniprocessor speed (MIPS)</td>
<td>1</td>
<td>200</td>
<td>2500</td>
<td>2.5K</td>
</tr>
<tr>
<td>CPUs per computer</td>
<td>1</td>
<td>1</td>
<td>10+</td>
<td>10+</td>
</tr>
<tr>
<td>Processor MIPS/$</td>
<td>$100K</td>
<td>$25</td>
<td>$0.20</td>
<td>500K</td>
</tr>
<tr>
<td>DRAM Capacity (MiB)/$</td>
<td>0.002</td>
<td>2</td>
<td>1K</td>
<td>500K</td>
</tr>
<tr>
<td>Disk Capacity (GiB)/$</td>
<td>0.003</td>
<td>7</td>
<td>25K</td>
<td>10M</td>
</tr>
<tr>
<td>Home Internet</td>
<td>300 bps</td>
<td>256 Kbps</td>
<td>20 Mbps</td>
<td>100K</td>
</tr>
<tr>
<td>Machine room network</td>
<td>10 Mbps (shared)</td>
<td>100 Mbps (switched)</td>
<td>10 Gbps (switched)</td>
<td>1000</td>
</tr>
<tr>
<td>Ratio of users to computers</td>
<td>100:1</td>
<td>1:1</td>
<td>1:several</td>
<td>100+</td>
</tr>
</tbody>
</table>

Anderson Dahlin 2014
People-to-Computer Ratio Over Time

• Today: Multiple CPUs/person!
  – Approaching 100s?

From David Culler

- Number Crunching
- Data Storage
- Productivity
- Interactive
- Streaming Information to/from physical world
• *Retail* hard disk capacity in GB

What is an Operating System?

Diagram showing the structure of an operating system, including layers such as User-mode, Kernel-mode, Hardware Abstraction Layer, and Hardware components.
What is an Operating System?

• **Referee**
  – Manage sharing of resources, Protection, Isolation
    • Resource allocation, isolation, communication

• **Illusionist**
  – Provide clean, easy to use abstractions of physical resources
    • Infinite memory, dedicated machine
    • Higher level objects: files, users, messages
    • Masking limitations, virtualization

• **Glue**
  – Common services
    • Storage, Window system, Networking
    • Sharing, Authorization
    • Look and feel
A Modern processor: SandyBridge

- Package: LGA 1155
  - 1155 pins
  - 95W design envelope
- Cache:
  - L1: 32K Inst, 32K Data (3 clock access)
  - L2: 256K (8 clock access)
  - Shared L3: 3MB – 20MB (not out yet)
- Transistor count:
  - 504 Million (2 cores, 3MB L3)
  - 2.27 Billion (8 cores, 20MB L3)
- Note that ring bus is on high metal layers – above the Shared L3 Cache
Functionality comes with SandyBridge I/O Configuration

- Proc
- Caches
- Memory
- Busses
- adapters
- Controllers
- I/O Devices:
  - Disks
  - Displays
  - Keyboards
- Networks
- Proc
- Caches
- Memory
- Busses
- adapters
- Controllers
- I/O Devices:
  - Disks
  - Displays
  - Keyboards
- Networks
• One application at a time
  – Had complete control of hardware
• Batch systems
  – Keep CPU busy by having a queue of jobs
  – OS would load next job while current one runs
• Multiple users on computer at same time
  – Multiprogramming: run multiple programs at seemingly at the “same time”
• Multiple processors in the same computer
Early processors, LC-3 is an example

- Instructions and data fetched from Main Memory using a program counter (PC)
- Traps and Subroutines
  - Obtaining address to branch to, and coming back
  - Using Stack Frames for holding
    - Prior PC, FP
    - Arguments and local variables
- Dynamic memory allocation and heap
- Global data
One Processor One program View

• External devices: disk, network, screen, keyboard etc.
• Device interface: Status and data registers
• User and Supervisor modes for processor
• I/O
  – Device drivers can use polling or interrupt
  – Interrupts need context switch
  – I/O done in supervisor mode
  – System calls invoke devise drivers

Enough info to resume
What introductory texts don’t include

• No cache
• Direct memory access (DMA) between Main Memory and Disk (or network etc)
  – Transfer by blocks at a time
• Neglecting the fact that memory access slower than register access
• Letting program run \textit{concurrently} (Multiprogramming) or with many threads
• Multiple processors in the system (like in Multicore)