

CS470 Spring 2008

Homework Assignment 1 Answers Due Feb. 12, 2008

Problem 1:

a. The truth table for a combinational circuit is given below with the inputs A, B and C and the outputs X, Y and Z. Obtain minimized expressions for X, Y and Z in sum-of-products form.

A	B	C	X	Y	Z
0	0	0	1	1	1
0	0	1	1	0	0
0	1	0	0	x	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	1	1	1
1	1	1	1	0	1

A \ B C	00	01	11	10
0	1	1	1	0
1	0	0	1	1

$$X = \bar{A}\bar{B} + BC + AB$$

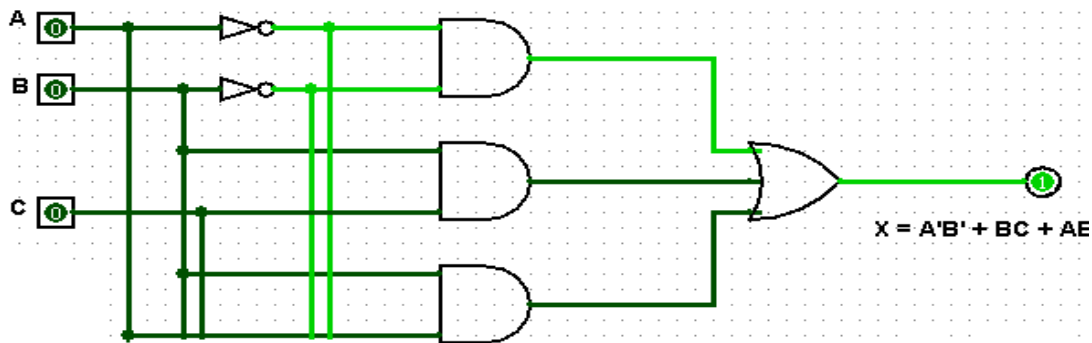
A \ B C	00	01	11	10
0	1	0	0	X
1	1	1	0	1

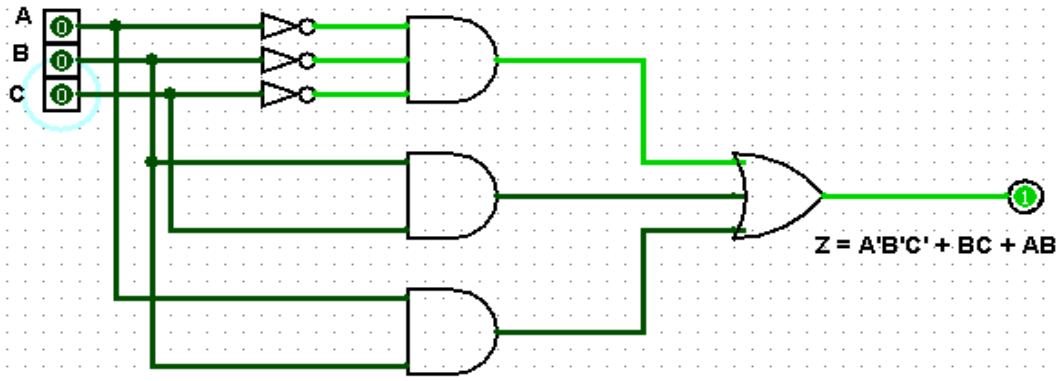
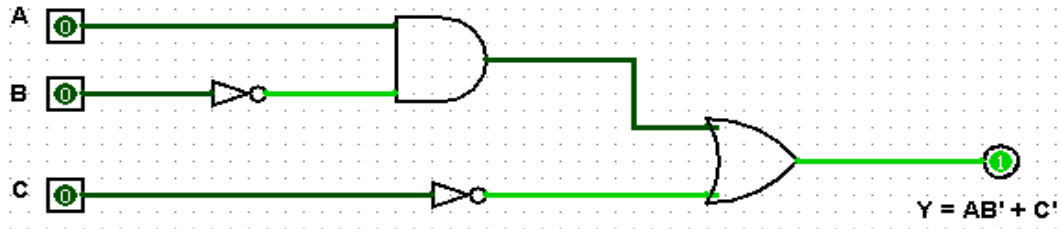
$$Y = A\bar{B} + \bar{C}$$

A \ B C	00	01	11	10
0	1	0	1	0
1	0	0	1	1

$$Z = \bar{A}\bar{B}\bar{C} + BC + AB$$

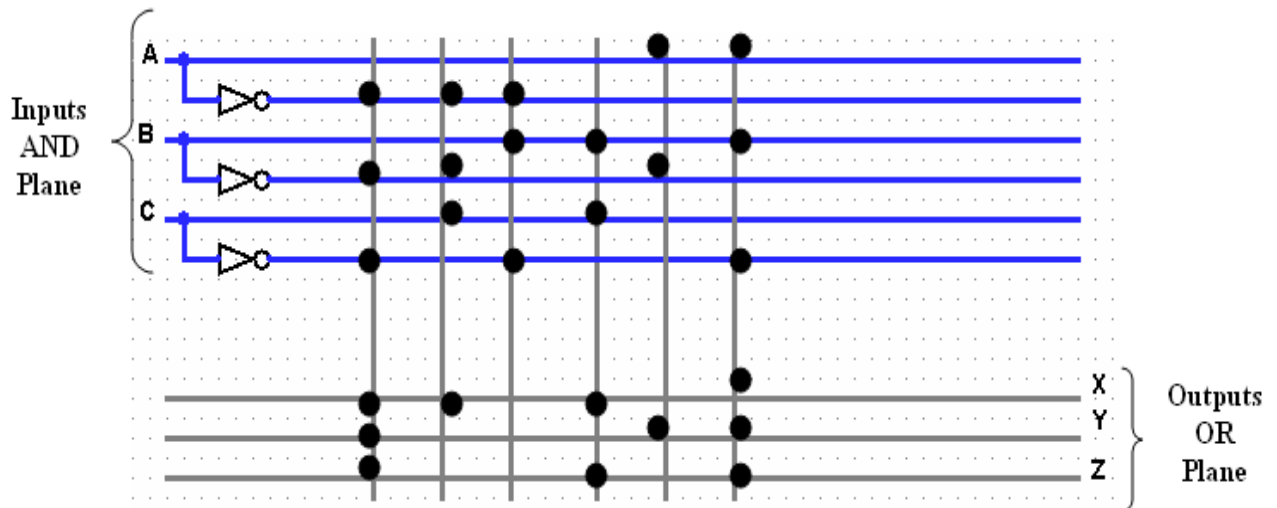
c. Give a logic diagram for both using AND gates, OR gates and inverters. Verify the design using Logisim (see lab assignment)





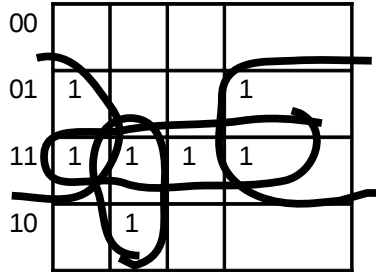
d. Implement the above function as a PLA. Minimize the number of product terms. Show the table as well as the PLA diagram.

A	B	C	X	Y	Z
0	0	0	1	1	1
0	0	1	1	0	0
0	1	0	0	X	0
X	1	1	1	0	1
1	0	X	0	1	0
1	1	0	1	1	1



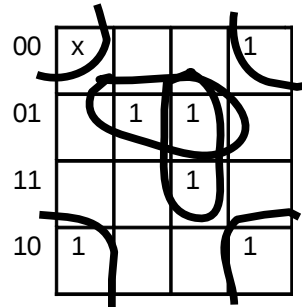
Problem 2: Obtain minimized SOP expressions.

AB\C 0 0 1
D 0 1 1 10

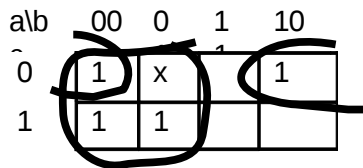


$$AB + A\bar{C}D + B\bar{D}$$

AB\C 0 0 1 1
D 0 1 1 0



$$\bar{B}\bar{D} + \bar{A}BD + BCD$$



$$\bar{B} + \bar{A}\bar{C}$$

Problem 3: Answer questions B.7 and B.9 from the text (Appendix B on CD). Minimize the PLA. (Use extra paper as needed).

	Inputs				Outputs
	A	B	C	D	F
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	1
4	0	0	1	1	0
5	0	1	0	0	1
6	0	1	0	1	0
7	0	1	1	0	0
8	0	1	1	1	1
9	1	0	0	0	1
10	1	0	0	1	0
11	1	0	1	0	0
12	1	0	1	1	1
13	1	1	0	0	0
14	1	1	0	1	1
15	1	1	1	0	1
16	1	1	1	1	0

Inputs					Outputs
	A	B	C	D	F
1	0	0	0	1	1
2	0	0	1	0	1
3	0	1	0	0	1
4	0	1	1	1	1
5	1	0	0	0	1
6	1	0	1	1	1
7	1	1	0	1	1
8	1	1	1	0	1

