

# Yashwant K. Malaiya

Computer Science Department  
Colorado State University  
Fort Collins, Colorado 80523  
malaiya@cs.colostate.edu

## 1 Education

Ph.D.	(Electrical Engineering)	Utah State University	1978
M.S.	(Electronics)	BITS, Pilani, India	1974
M.S.	(Physics)	Saugor University, India	1971
B.S.	(Physics, Math)	GD College, Damoh, MP, India	1969

## 2 Experience

1990-: Professor, Computer Science Dept.

1982-90: Associate Professor, Computer Science Dept., Colorado State University

1978-82: Assistant Professor, Dept. of Computer Science, State Univ. of New York at Binghamton

## 3 Areas of research emphasis

Quantitative Security, Reliability, Fault modeling and testing, Testable and Fault-tolerant digital design

## 4 Professional Activities

### 4.1 Conferences

- General Chair, IEEE International Symposium on Software Reliability Engineering (ISSRE), Denver, 2003.
- General Co-Chair, IEEE Asian Test Symposium, Shanghai, 1999.
- General Chair, The Fourth International Symposium on Software Reliability Engineering (ISSRE), Denver, Nov. 1993.
- General Chair, Sixth International Conference on VLSI Design (VLSI Design '93), Bombay, India, 1993.
- Program Chair, Fifth International Conference on VLSI Design (VLSI Design '92), Bangalore, India, 1992.
- General Chair, 24th ACM/IEEE International Symposium on Microarchitecture (Micro-24), Albuquerque, 1991.
- General Chair, IEEE International Workshop on IDDQ Testing (IDDQ-95), Washington D.C., October 1995, 2000.
- Chair Steering Committee, IEEE International Workshop on IDDQ Testing, 1996, 1997.
- Program Co-Chair, The Eighth International Symposium on Software Reliability Engineering (ISSRE), Albuquerque, Nov. 1997.
- IEEE liaison for International Conference on VLSI Design 1994-1998.

### 4.2 Editing

- Guest editor, IEEE Software, Special issue on Reliability Measurement, July 1992, with P. Srimani.
- Guest Editor, IEEE Design & Test, Special issue on VLSI Design, Dec. 1992.
- Editor, MicroArch, Quarterly publication of IEEE CS TC on Microprogramming and microarchitecture (1989-93)
- Digest of Papers - IEEE International Workshop on IDDQ Testing, Washington D.C., Oct. 1995.

- Editor-in-Chief, Journal of Software Engineering and Applications, 2011-2012.

### 4.3 Organizations

- Commissioner, ABET Computing Accreditation Commission, 2005
- Evaluator, Computing Sciences Accreditation Board, 1999-continuing.
- Member Editorial Board, Intelligent Information management, 2010-
- **PC member:** ICQRMS 2011, ISSRE 2010, etc.
- Vice chair, **IEEE CS Award Committee (1995-99)** (Service Awards).
- Vice Chair, **TCSE Software Reliability Engineering Committee** (1990-96).
- Chair, **Test Technology TC Subcommittee on Software Testing**, (1993-2002).
- Member, Executive Committee, IEEE CS Technical Activities Board (1988-98); IEEE CS Conference and Tutorials Board (1994, 2000, 2001);
- Chair, **IEEE-CS Technical Committee on Microprogramming and Microarchitecture**, (1988-92).
- Senior Member IEEE Computer Society.

## 5 Reviewer

- **Journals** : IEEE Trans. Computers, IEEE Trans. Reliability, IEEE Trans. Software Engineering, IEEE Software, IEEE Trans. CAD, IEEE Journal of Solid State Circuits, IEEE Trans. VLSI Systems, IEEE Design and Test, IEEE Trans on Systems, Man, and Cybernetics, Software Process: Improvement and Practice, Software Quality Journal, Empirical Software Engineering, Software Testing, Verification and Reliability, Journal of Digital Systems, Journal for Electronic Testing, Naval Research Logistics Quarterly, IEE Electronic Letters, IET Software, Int. Journal of Software Engineering,
- **Conferences** : Int. Symp. on Software Reliability Engineering, International Symposium on Fault-tolerant Computing, International Test Conference, Design Automation Conference, IEEE Tencon, Int. Symp. and Work. on Microprogramming and Microarchitecture, Asian Test Symposium, VLSI Design, IEEE/IFIP Int Conference on Embedded & Ubiquitous Computing etc.
- **Funding Agencies** : National Research Council, NSF, Research Grants Council, Hong Kong, Uberoi foundation.
- **Publishers** : Computer Science Press, West Educational Publishing, John Wiley, McGraw-Hill, Asken.
- **External Reviewer for Universities** : Roorkee University, State University of New York, Georgia Tech, University of Wyoming, Florida Atlantic University, Chinese University of Hong Kong, West Virginia State.

## 6 Courses

Graduate: Fault-Tolerant Computing, Testable Systems, Advanced Fault-Tolerant Computing

Undergraduate: Logic Design, Computer Organization and Assembly Language, Computer Architecture, Interactive Programming with Java, Microprogramming and bit-sliced devices, Microcomputer programming and interfacing, Discrete structures, Data Communications

## 7 Recognitions

- IEEE CS Certificate of Appreciation, 2003, "for exceptional effort as General Chair in organizing and running a successful ISSRE 2003".
- IEEE CS Meritorious Service Award, 2002 "For providing skilled management and guidance to the IEEE International Workshop on Defect Based Testing for over five years".
- IEEE Third Millennium Medal, 2000.
- Best Paper Award, ISSRE 1997 (see Publications).
- IEEE CS Golden Core Award, June 1996.
- IEEE CS Certificate of Appreciation Award, Oct. 20, 1996 "*For significant leadership contribution to the International IDDQ Test Workshop as Chairman, 1995*"
- IEEE CS Meritorious Service Award, Feb. 1993. *For Tecgnical and administrative leadership while serving as Chair of the Technical Committee on Microprogramming and Microarchitecture*

- Honorary appointment as Professor, Electrical Eng. Dept., CSU.
- Invited lectures at China Academy of Sciences, Beijing, and Shanghai University of Science and Technology (3 weeks), 1989.
- Merit List, University of Saugor, 1971.
- Rotary Club Award: Top B.Sc. student, GD College, Damoh, 1969.
- Sanskrit Scholarship, GMHS School, Damoh, 1963-66.
- Named in *American Men and Women of Science*.

## Publications

### 1 Books/Chapters:

1. Y. K. Malaiya, "Optimal Reliability Allocation," **Wiley Encyclopedia of Operations research and Management Science**, John Wiley & Sons, Jan. 2011.
2. Y.K. Malaiya, "Software Reliability Management," **Encyclopedia of Library and Information Sciences**, Taylor and Francis, Editor: S. Lee, Third Edition, 1: 1, 4901 — 4912, February 2010.
3. Y. K. Malaiya, "Reliability Allocation," **Encyclopedia of Statistics in Quality and Reliability**, John Wiley & Sons, March 2008, 5 pages.
4. Y. K. Malaiya, "Software Reliability and Security," in **Encyclopedia of Library and Information Science**, 2005. Y.K. Malaiya,
5. "Software Reliability", **Encyclopedia of Library and Information Science**, Editors: A. Kent and C.M. Hall, Pub. Marcel Dekker, Inc. 2003, pp. 2688 - 2698.
6. Y.K. Malaiya, "Software Reliability", **Encyclopedia of Library and Information Science**, Editors: A. Kent and C.M. Hall, Pub. Marcel Dekker, Inc. V. 67, May 2000, pp. 341-357.
7. Y.K. Malaiya, "Automated Test Software", for **Wiley Encyclopedia of Electrical and Electronics Engineering**, Editor: J.G. Webster, Pub. John Wiley & Sons, Inc. 1999, pp. 135-141.
8. Karunanithi and Y.K. Malaiya, "Neural Networks for Software Reliability", Chapter in **Handbook on Software Reliability Engineering**, Ed. M. Lyu, Publisher: McGraw-Hill, 1996. 108. 1
9. Y.K. Malaiya, "Golapurva Anvaya: Eksa Parichaya" (Hindi), in **Golapurva Jain Samaj: Itihas evam Sarvekshana** ed. Dr. Surendra K. Jain, Pub. Paras Research Inst., Sagar, 1996, pp. 32-44.
10. C.C. Liaw, S.Y.H. Su and Y.K. Malaiya, "Test Generation for Delay Faults using Stuck-at Fault Test Set," **25<sup>th</sup> Anniversary Compendium of papers**, International Test Conference, 1994, pp. 206-214 (selected for republication).
11. **Bridging Faults and IDDQ Testing**, Editors: Y.K. Malaiya and R. Rajsuman, *IEEE Computer Society Press Technology Series*, 1992.
12. **Software Reliability Models: Theoretical Development, Evaluation and Applications**, Editors: Y.K. Malaiya and P. Srimani, *IEEE Computer Society Press Technology Series*, 1990.
13. Y.K. Malaiya, "Identification of Golladesh and Gollacharya on the basis of Kuvalayamala-kaha," in **Jaganmohanlal Shastri Felicitation Volume**, JML Sadhuvad Samiti, 1990 (in Hindi) pp. 448-454.
14. Y.K. Malaiya, "On the Golapurva Caste" in **Vyakaranacharya Banshidhar Felicitation Volume**, 1990 (in Hindi), pp. 103-130.
15. C.C. Liaw, S.Y.H. Su and Y.K. Malaiya, "Test Generation for Delay Faults using Stuck-at Fault Test Set," **VLSI Support Technologies: Computer-Aided Design, Testing and Packaging**, Ed. Rex Rice, IEEE Computer Society Press, 1982, pp. 281-290 (selected for republication).

### 2 Patents

1. W.K. AlAssadi, A.P. Jayasumana and Y.K. Malaiya, "IDDQ Testing of Integrated Circuits" Patent granted May 26, 1998.

### 3 Software Tools

1. **ROBUST**, *An integrated Software Reliability tool*. MS Windows, X-Windows, <http://www.cs.colostate.edu/testing/robust/>.

### 4 Journals

- 1 S.-W. Woo, H. Joh, O. H. Alhazmi and Y. K. Malaiya, "Modeling Vulnerability Discovery Process in Apache and IIS HTTP Servers", *Computers & Security*, Vol. 30, Issue 1, 2011, pp. 50-62.
- 2 S.H. Wu, S. Jandhyala, Y. K. Malaiya, A. P. Jayasumana, "Antirandom Testing: A Distance Based Approach," *VLSI Design*, 2008, 9 pages, 2008. doi:10.1155/2008/165709.
- 3 O. H. Alhazmi and Y. K. Malaiya, "Application of Vulnerability Discovery Models to Major Operating Systems," *IEEE Trans. Reliability*, March 2008, pp. 14-22.
- 4 Y. K. Malaiya, "Giants from the Annals of Jain History", *Jinamanjari*, 37.1, 2008, 3-29.
- 5 O. H. Alhazmi, Y. K. Malaiya , I. Ray, " Measuring, Analyzing and Predicting Security Vulnerabilities in Software Systems," *Computers and Security Journal*, Volume 26, Issue 3, May 2007, Pages 219-228.
- 6 Y.K. Malaiya, N. Li, J. Bieman, R. Karcich, "Software Test Coverage and Reliability," *IEEE Trans. Reliability*, Dec. 2002, pp. 420-426.
- 7 Y.K. Malaiya, "Kundalpur's Past Three Centuries," *Arhat Vacan*, Vol. 13, no. 3-4, 2001 pp. 5-13.
- 8 S.M. Menon, Y.K. Malaiya, A.P. Jayasumana and C.Q. Tong, "Operational and Test Performance in the Presence of Built-in Current Sensors," *Int. Journal of VLSI Design*, 1997, V. 5, No. 3, pp. 285-298.
- 9 S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "ECL Storage Elements: Modeling of Faulty Behavior," *IEEE Trans. Circuits & Systems-II*, Nov. 1997, pp. 970-974.
- 10 M. Menon, A. P. Jayasumana and Y. K. Malaiya, "BiCMOS Domino: A Novel High-Speed Dynamic BiCMOS Logic," *Int. Journal of Electronics*, 1997, V. 83, No. 2, pp. 177-189.
- 11 S.M. Menon, A.P. Jayasumana and Y.K. Malaiya "Testable Design for BiCMOS Stuck-Open Fault Detection using Single Patterns" *IEEE Journal of Solid State Circuits*, Aug. 1995, pp. 855-863.
- 12 S.M. Menon, A.P. Jayasumana and Y.K. Malaiya, "Manifestation of Faults in Single and Double BJT BiCMOS Logic Gates," *Proc. IEE, Pt. E, Computers and Digital Techniques*, Vol. 142, No. 2, pp. 135-144, March 1995.
- 13 Y.K. Malaiya, A.P. Jayasumana, Q. Tong and S. Menon, "Resolution Enhancement in IDDQ testing for Large ICs" *International Journal of VLSI Design*, Vol. 1, No. 4, pp. 277-284.
- 14 N. Karunanithi, D. Whitley and Y.K. Malaiya, "Prediction of Software Reliability using a Connectionist Approach," *IEEE Trans. Software Engineering*, Sept. 1992, pp. 563-574.
- 15 Y.K. Malaiya, "Golahivai and Golladeshadhipa" *Arhat-Vachan*, 1994 (in Hindi).
- 16 W.K. Al-Assadi, D. Lu, A.P. Jayasumana, Y.K. Malaiya and C.Q. Tong, "Data Feed-through Faults in circuits using Unclocked Storage Elements," *Electronic Letters*, Vol. 30, No. 10, May 12, 1994, pp. 764-765.
- 17 Y.K. Malaiya, A. von Mayrhauser and P. Srimani, "An Examination of Fault Exposure Ratio," *IEEE Trans. Software Engineering*, Nov. 1993, pp. 1087-1094.
- 18 S.M. Menon, A.P. Jayasumana, Y.K. Malaiya and D.R. Clinkinbeard, "Modeling and Analysis of Bridging Faults in Emitter-Coupled Logic (ECL) Circuits," *IEE Proceedings, Computer and Digital Techniques*, Vol. 140, No. 4, July 1993, pp. 220-226.
- 19 W. Alassadi, Y.K. Malaiya and A.P. Jayasumana, "Faulty Behavior of Storage Elements and its Effects on Sequential Circuits" *IEEE Trans. VLSI Systems*, Dec. 1993 pp. 446-452.
- 20 Y.K. Malaiya, "The Sravakas of Madanasagarpura in the Chandel Period" *Anekanta*, July-Sept. 1993 (in Hindi).
- 21 Y.K. Malaiya, N. Karunanithi and P. Verma, "Predictability of Software Reliability Models," *IEEE Trans. Reliability*, Dec. 1992, pp. 539-546.
- 22 N. Karunanithi, D. Whitley and Y.K. Malaiya, "Applying Neural Networks to Software Reliability Prediction," *IEEE Software*, July 1992, pp. 53-59.
- 23 Y. Min, Y.K. Malaiya and B. Jin, "Analysis of Detection Capability of Parallel Signature Analyzers," *IEEE Trans. Computers*, Vol. 40, No. 9, Sept. 1991, pp. 1075-1081.
- 24 A.P. Jayasumana and Y.K. Malaiya and R. Rajsuman, "Design of CMOS Circuits for Stuck-Open Fault Testability," *IEEE Journal of Solid State Circuits*, Vol. 26, No.1, January 1991, pp. 58-61.
- 25 A.P. Jayasumana, W. Al-assadi and Y.K. Malaiya, "On Pass Transistor Logic Design," *International Journal of Electronics*, Vol. 70, No. 4, April 1991, pp. 739-749.

- 26 S. Feng and Y.K. Malaiya, "Optimization of Test Parallelism with Limited Hardware Overhead," *Microelectronics and Reliability*, Vol. 31, No. 2, 1991, pp. 271-276.
- 27 Y.K. Malaiya, "The Sravakas of Golladesh and Gollapura," *Anekanta*, Vol. 44, No. 1, Jan. 1991, pp. 4-8 (in Hindi).
- 28 Y. Min, Y.K. Malaiya and B. Jin, "Aliasing errors in parallel signature analyzers," *Journal of Computer Science and Technology*, V. 5, No. 1, January 1990, pp. 25-40.
- 29 S.M. Menon, A.P. Jayasumana and Y.K. Malaiya, "Fault Modeling for ECL Devices," *Electronic Letters*, Vol. 26, NO. 15, July 19, 1990, pp. 1105-1108
- 30 R. Rajsuman, Y.K.Malaiya and A.P. Jayasumana, "Reprogrammable FPLA with Universal Test Set," *Proc. IEE*, Vol. 137, Pt. E, No. 6, Nov. 1990, pp 437-441.
- 31 R. Rajsuman, Y.K. Malaiya and A.P. Jayasumana, "Limitations of Switch Level Analysis for Bridging Faults," *IEEE Trans. CAD.*, Vol. 8, No. 7, July 1989, pp. 807-811.
- 32 R. Rajsuman, A.P. Jayasumana and Y.K. Malaiya, "CMOS Stuck-open Fault Detection in Presence of Glitches and Timing Skews," *IEEE Journal of Solid State Circuits*, Vol. 24, No. 4, August 1989, pp. 1055-1061.
- 33 R. Rajsuman, Y.K. Malaiya and A.P. Jayasumana, "CMOS Stuck-open Fault Testability," *IEEE Journal of Solid State Circuits*, Vol. 24, No. 1, pp. 193-194, Feb. 1989.
- 34 Y. Min, Y.K. Malaiya and B. Gupta, "On the Computational Complexity of Test Generation for ETG PLAs," *IEE Proceedings* Vol. 136, Pt. E, No. 2, March 1989, pp. 107-111.
- 35 R. Rajsuman, A.P. Jayasumana and Y.K. Malaiya, "On Testing of Complex Gates," *Electronic Letters*, Vol. 23, No. 16, July 30, 1987, pp. 813-814.
- 36 Y.K. Malaiya, "Analyzing Data for CMOS Leakage Faults," *Microelectronics and Reliability*, Vol. 25, No. 5, 1985, pp. 943-948.
- 37 Y.K. Malaiya and R. Narayanaswamy, "Modeling and Testing for Timing Faults in Synchronous Sequential Circuits," *IEEE Design and Test of Computers*, Vol. 1, No. 4, November 1984, pp. 62-74.
- 38 Y.K. Malaiya and S.Y.H. Su, "Analysis of an Important Class of Non- Markov Systems," *IEEE Trans. Reliability*, Vol. R-31, No. 1, April 1982, pp. 64-68.
- 39 Y.K. Malaiya, "Linearly Correlated Intermittent Failures," *IEEE Trans. Reliability*, Vol. 31, No. 2, June 1982, pp. 211-215.
- 40 Y.K. Malaiya and S.Y.H. Su, "Reliability Evaluation for Hardware Redundancy Fault-Tolerant Systems with Intermittent Faults," *IEEE Trans. Computers*, Vol. C-30, No. 8, August 1981, pp. 600-604.
- 41 C.C. Liaw, S.Y.H. Su and Y.K. Malaiya, "Test-Experiments for Detection and Location of Intermittent Faults in Sequential Circuits," *IEEE Trans. Computers*, Vol. C-30, No. 12, December 1981, pp. 989-995.
- 42 S.Y.H. Su, I. Koren, Y.K. Malaiya, "A Continuous Parameter Markov Model and Detection Procedures for Intermittent Faults," *IEEE Trans. Computers*, Vol. C-27, No. 6, June 1978, pp. 567-570.
- 43 Y.K. Malaiya, "An Examination of the Sixteenth Chapter of Vardhamana Purana," *Anekanta*, Vol. 27, No. 2, August 1974, pp. 58-64 (in Hindi).
- 44 Y.K. Malaiya, "On the Golapurvas," *Anekanta*, Vol. 25, No. 2, May 1972, pp. 68-72 (in Hindi).
- 45 Y.K. Malaiya, "Research Notes," *Anekanta*, Vol. 24, No. 5, November 1971, pp. 213-214 (in Hindi).

## 5 Conferences

1. H. Joh and Y. K. Malaiya, "Defining and Assessing Quantitative Security Risk Measures Using Vulnerability Lifecycle and CVSS Metrics," Proc. Int. Conference on Security and Management (SAM11), 2011, pp.10-16.
2. A. A. Younis, H. Joh, and Y. K. Malaiya, "Modeling Learningless Vulnerability Discovery using a Folded Distribution," Proc. Int. Conference on Security and Management (SAM11), 2011.
3. HyunChul Joh and Yashwant K. Malaiya, "A Framework for Software Security Risk Evaluation using the Vulnerability Lifecycle and CVSS Metrics" International Workshop on Risk and Trust in Extended Enterprises (RTEE'2010), November 2010, pp. 430-434.
4. X. He, Y. K. Malaiya, A. P. Jayasumana, K. P. Parker and S. Hird, "Principal Component Analysis-Based Compensation for Measurement Errors Due to Mechanical Misalignments in PCB Testing" Proc. 41st International Test Conference (ITC'10), Austin, Texas, November 2010, pp.16.1.1-10.
5. H. Joh and Y. K. Malaiya, "Modeling Skewness in Data with S-shaped Vulnerability Discovery Models" Proc. Int. Symp. Software Reliability Eng. (ISSRE), Fast Abstracts, November 2010, pp. 406-407.

6. H. Joh, S. Chaichana and Y. K. Malaiya, "Short-term Periodicity in Security Vulnerability Activity" Proc. Int. Symp. Software Reliability Eng. (ISSRE), Fast Abstracts, November 2010, pp. 408-409.
7. A. P. Jayasumana, Y. K. Malaiya, X. He, K. P. Parker and S. Hird, "Compensation for measurement errors due to mechanical misalignment in PCB testing," IEEE 9th International Board Test Workshop (BTW'10), Fort Collins, CO, Sept. 14 - 16, 2010.
8. X. He, Y. K. Malaiya, A. P. Jayasumana, K. P. Parker and S. Hird, "An Outlier Detection Based Approach for PCB Testing," Proc. IEEE Int. Test Conference, Nov. 2009, pp. 1-10.
9. X. He, Y. Malaiya, A. P. Jayasumana, K. P. Parker and S. Hird, "Outlier Detection in Capacitive Open Test Data Using Principal Component Analysis," Presented at the IEEE 8th International Board Test Workshop (BTW'09), Fort Collins, CO, Sept. 2009.
10. H. Joh and Y. K. Malaiya, "Seasonal Variation in the Vulnerability Discovery Process," Proc. 2nd IEEE Int. Conf. Software Testing, Verification, and Validation, April 2009, pp. 191-200.
11. H. Joh and Y. K. Malaiya, "Seasonality in Vulnerability Discovery in Major Operating Systems and Web Applications," Fast Abstract, Proc. Int. Symp. Software Reliability Eng., Nov. 2008, pp. 297-298.
12. H. Joh, J. Kim and Y. K. Malaiya, "Vulnerability Discovery Modeling using Weibull Distribution," Fast Abstract, Proc. Int. Symp. Software Reliability Eng., Nov. 2008, pp. 299-300.
13. J. Kim, Y. K. Malaiya and I. Ray, "Vulnerability Discovery in Multi-Version Software Systems," Proc. 10th IEEE Int. Symp. on High Assurance System Engineering (HASE), Dallas, Nov. 2007, pp. 141-148.
14. A. Sanyal, A. Sokolov, Y. Malaiya and D. Whitley, "A Co-evolutionary Algorithm for Dynamic Power Minimization During Scan Testing," 16th IEEE North Atlantic Test Workshop, May 2007, pp. 13-18.
15. Jinyoo Kim, Omar Alhazmi and Yashwant Malaiya, "Vulnerabilities in Browsers: Trends in Internet Explorer and Firefox", Supp. Proc. ISSRE Fast Abstracts, Nov. 2006, pp 1-2.
16. S-W. Woo, O.H. Alhazmi and Y.K. Malaiya, "An Analysis of the Vulnerability Discovery Process in Web Browsers", Proc. 10th IASTED Int. Conf. on Software Engineering and Applications, Nov. 2006.
17. O.H. Alhazmi and Y.K. Malaiya, "Measuring and Enhancing Prediction Capabilities of Vulnerabilities Discovery Models for Apache and IIS HTTP Servers ", Proc. Int. Symp. Software Reliability Eng, Nov. 2006, pp. 343-352.
18. O.H. Alhazmi, S-W. Woo, and Y.K. Malaiya, "Security Vulnerability Categories in Major Software Systems", Proc. IASTED Int. Conference on Communication, Network and Information Security, Oct. 2006. pp.138-143.
19. S-W. Woo, O.H. Alhazmi and Y.K. Malaiya, "Assessing Vulnerabilities in Apache and IIS HTTP Servers", Proc. IEEE Int. Symp. on Dependable, Autonomic and Secure Computing (DASC'06), Sept.-Oct. 2006, pp. 103-110.
20. A. Sharma, A. P. Jayasumana and Y.K. Malaiya, "X-IDDQ: A Novel Defect Detection Technique using IDDQ Data," Proc. IEEE VLSI Test Symposium, April-May 2006, pp. 180-185.
21. O. H. Alhazmi and Y. K. Malaiya, "Prediction Capabilities of Vulnerability Discovery Models," Proc. Reliability and Maintainability Symposium, Jan 2006, pp.86-91.
22. O. H. Alhazmi and Y. K. Malaiya, "Modeling the Vulnerability Discovery Process," Proc. Int. Symp. Software Reliability Eng, Nov. 2005, pp. 129-138.
23. Y. K. Malaiya, C. Braganza and C. Sutaria, "Early Applicability of the Coverage/Defect Model," Supp. Proc. Int. Symp. Software Reliability Eng, Nov. 2005, pp. 4.27-4.28.
24. A. Sokolov, A. Sanyal, D. Whitley, Y.K. Malaiya, "Dynamic Power Minimization During Combinational Circuit Testing as a Traveling Salesman Problem," Proc. 2005 IEEE Congress on Evolutionary Computation, Sept. 2005, pp. 1088-1095.
25. O. H. Alhazmi, Y. K. Malaiya and I. Ray, "Security Vulnerabilities in Software Systems: A Quantitative Perspective," Proc. IFIP WG 11.3 Working Conference on Data and Applications Security, August 2005, pp. 281-294.
26. A. S. Banthia, A. P. Jayasumana and Y. K. Malaiya, "Data Size Reduction for Clustering Based Binning of ICs Using Principal Component Analysis (PCA)", Proc. IEEE Int. Workshop on Defect Based Testing, May 2005., pp. 27-33.
27. O. Alhazmi, Y.K. Malaiya, "Quantitative Vulnerability Assessment of System Software," Proc. IEEE Reliability and Maintainability Symposium, Jan. 2005, pp. 615-620.
28. J. Chen and Y.K. Malaiya, "Augmenting Test Case Generation using Statechart," Proc. Int. Conf. Software Eng. Research and Practice, June 2004, pp. 608-614.
29. D. Henry and Y.K. Malaiya, "A Visualization System for Sliding Windows Protocol," Proc. ACM/IEEE Frontiers in Education Conference, Nov. 2003, pp. T2C1-T2C6.
30. R.P. Turakhia, A.P. Jayasumana and Y.K. Malaiya, "Clustering based Production Line binning of ICs based on

- IDDQ,” *Proc. Int. Work. on Defect Based Testing*, April 2003, pp. 65-73.
31. H.V. Kantamneni, S.R.Pillai and Y.K. Malaiya “Structurally Guided Testing,” in *Supp. Proc. Int. Symp. Software Reliability Eng.*, Nov 2002, pp. 137-138.
  32. R.Ye and Y.K. Malaiya, “Relationship between test effectiveness and Coverage,” in *Supp. Proc. Int. Symp. Software Reliability Eng.*, Nov 2002, pp. 159-160.
  33. Rao, A.P. Jayasumana and Y.K. Malaiya “Optimal Clustering and Statistical Identification of Defective ICs using IDDQ Testing,” *Proc. IEEE Int Work. on Defect Based Testing*, April 2000, pp. 30-35.
  34. Y. K. Malaiya and J. Denton “Module Size Distribution and Defect Density,” *Proc. IEEE International Symposium on Software Reliability Engineering*, Oct. 2000, pp. 62-71.
  35. Y. K. Malaiya and J. Denton “Requirement Volatility and Defect Density,” *Proc. IEEE Int. Symp. Software Reliability Engineering*, Nov. 1999, pp. 285-294.
  36. Palaniswamy, A. Jayasumana Y. K. Malaiya “A Neural Network based Approach for Testing Analog Circuits with Frequency Domain Classification and Time Domain Testing”, *Int. Work. on System Test Diagnosis*, 1999.
  37. S.H. Wu, Y.K. Malaiya and A.P. Jayasumana, “Antirandom vs. Psuedorandom Testing” *Proc. IEEE International Conference on Computer Design*, Oct. 1998.
  38. M.N. Li, Y.K. Malaiya and J. Denton, “Estimating the Number Defects: A Simple and Intutive Approach” *Proc. IEEE International Symposium on Software Reliability Engineering, Industrial Practices*, November 1998, pp. 307-315.
  39. Y.K. Malaiya and J. Denton, “Estimating the Number of Residual Defects” *Proc. IEEE High Assurance Systems Engineering Symposium (HASE '98)*, November 1998, pp. 98-105.
  40. Y. K. Malaiya and J. Denton, “What Do the Software Reliability Growth Model Parameters Represent?” *Int. Symp. on Software Reliability Engineering*, 1997. pp. 124-135.
  41. H. Yin, Z. Lebne-Dengel and Y. K. Malaiya, “Automatic Test Generation using Checkpoint Encoding and Antirandom Testing” *Int. Symp. on Software Reliability Engineering*, 1997, pp. 84-95. Best Paper Award.
  42. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, “Input Pattern Classification for Detection of Stuck-on and Bridging Faults Using IDDQ Testing in BiCMOS and CMOS Circuits,” *Proc. International Conference on VLSI Design*, Jan.1997, pp. 545-546.
  43. S. M. Menon, A. P. Jayasumana and Y. K. Malaiya, “Input pattern classification for transistor level testing of bridging faults in BiCMOS circuits,” *Proc. IEEE 6th Great Lakes Symposium on VLSI*, March 1996, pp. 214-219.
  44. N. Li and Y.K. Malaiya, “Fault Exposure Ratio: Estimation and Applications” *Proc. IEEE Int. Symp. Software Reliability Engineering*, 1996, pp. 372-381.
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2. "Modeling, Testing and Reliability Analysis of Digital Systems with Intermittent Faults," Ph.D. Dissertation, Department of Electrical Engineering, Utah State University, Logan, 155 pages, 1978.

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5. "Identification and Binning of Faulty ICs Using Principal Component Analysis," A. Sharma, A.P. Jayasumana and Y.K. Malaiya, 2005.

## **Graduate committees (since 2003 only)**

I have **advised more than 65** graduate students and have **served on the committees for more than 250** graduate students at Colorado State University. The list below is from 2003 only.

Ph.D.(as advisor/coadvisor) : Omar Alhazmi, HyunChul Joh, Sopak Chaichana, John Fan, Awad Younis.

Ph.D.(as committee member) : Fahad Al Zahrani, Zhou Dacheng, Abdulgader Habibulla, Alkan Cengiz, Ayman Fayumi, C.R. Rose, Dan Vivanco, Dinh Trong Trung, H Nasser, Huxia Wang, Nischal Piratla, J S Tamez, Pan Ho Lee, Henry Dittmer, Sudip Chakraborty, Woo Sung-whan, Sangeeta Bangalore, Yoong Goog Cho.

M.S. (as advisor/coadvisor): Abraham Daniel, Jiao Chen, Kishore Siddha Reddy, Sai Balbhadrapatruni, Sung-Whan Woo, Jinyoo Kim, Manja Prasanna, V R Parakala, Chinmay Gupte, Ritesh Turakhia, Ashutosh Sharma, Udaya Sajja.

M.S. (as committee member): Shenghong Fu, Priyanka R. Dumbre, Alodeep Sanyal, Vaibhav Nawale, Aditya Maroo, Kranthi Bodepudi, B Kumaraswami, Mageshkumar Kuppusamy, Michael Steigerwald, Ramanathan Sivakumar, Sudha Govindaswamy, Mehak Chopra, Supriya Sukumaran, Gerald Esch, Rohit Joshi, Praveen Moses, Sonja Tideman, Vinil Vargese, Ashish Mehta.