DBT-2005: IEEE International Workshop on Defect Based Testing

May 1, 2005 Lodge at Rancho Mirage, Palm Springs, CA, USA

Realizing Defect-Based Test in Production Test Flows

One of the fundamental questions in the testing community is the effectiveness of defect-based testing approaches in the production test flow. Defect-based testing has the potential to better handle emerging defect types and changing circuit sensitivities in VDSM circuits compared to conventional stuck-at (structural) test. Nevertheless, we need to better understand how many and which types of defects can be uniquely detected only by defect-based test techniques. However, some of the unique detections performed by defect-based testing can be just due to the lack of thorough structural test, such as untested faults or un-modeled faults. Data, experience, and lessons learned from the test floor regarding the application of DBT in a production test flow are essential to answer this question. Another issue is the problem of performing defect-based test in a foundry environment. This problem is pronounced for smaller companies in which the appropriate information flow between the companies and their foundries is crucial for performing defect-based test.

The IEEE International Workshop on **Defect Based Testing (DBT 2005)** is aimed at addressing these issues by providing an informal forum for the discussion of key recent advances and open research issues relating to defect based testing and associated test methodologies. The theme of this year's workshop **"Realizing Defect-Based Test in Production Test Flows"** has been selected to generate active discussion on the challenges that must be met to ensure high IC product quality through to the end of the decade.

PROGRAM

7:30-8:30 Registration

8:30-8:45 Welcome & Program Introduction
Sankaran Menon, General Chair
Hans Manhaeve, Co-General Chair
Jim Plusquellic, Vice-General Chair
Mehdi Tahoori, Program Chair

8:45-9:30 Keynote Address - 1: **Chuck Hawkins**, **ECE Dept., University of New Mexico, USA**
"**We are at the Next Test Paradigm & Other Topics**"

9:30-9:40 **Short Break**

9:40 - 10:40 Session 1: IDDX Applications & Monitor Design - 1 (Session Chair: Martin Margala, University of Rochester, USA)

9:40 - 10:00 Dhruva Acharyya, Abhishek Singh, Mohammad Tehanipoor, Chintan Patel and Jim Plusquellic, "***Sensitivity Analysis of Quiescent Signal Analysis for Defect Detection***"

10:00 - 10:20 Bin Xue and D. M. H. Walker, "***Technology Scaling Issues of an IDDQ Built-In Current Sensor***"

10:20 - 10:40 C. Thibeault, "***On the Test Quality Evaluation of Current Testing Techniques***"

10:40-11:00: **Short Break**

11:00 - 12:20 Session 2: Defect Data Analysis (Session Chair: Ali Chehab, American University of Beirut, Lebanon)

11:00 - 11:20 Ashish S. Banthia, Anura P. Jayasumana and Yashwant K. Malaiya, "***Data Size Reduction for Clustering Based Binning of ICs Using Principal Component Analysis (PCA)***"

11:20 - 11:40 Mariane Comte, Satoshi Ohtake, Hideo Fujiwara and Michel Renovell, "***Electrical Analysis of a Domino Logic Cell with GOS Faults***"

11:40 - 12:00 Piet Engelke, Valentin Gherman, Ilia Polian, Yuyi Tang, Hans-Joachim Wunderlich and Bernd Becker, "***Sequence Length, Area Cost and Non-Target Defect Coverage Tradeoffs in Deterministic Logic BIST***"

12:00 - 12:20 Rosa Rodríguez-Montañés and Joan Figueras, "***Electrical and Topological Characterization of Interconnect Open Defects***"

12:20-1:30 Lunch

1:30-2:15 Keynote Address - 2: Anne Gattiker, IBM Austin Research Laboratory, USA.
"Defects Yesterday, Today and Tomorrow: Implications for Test"

2:15 - 2:30 Short Break

2:30 - 3:30 Session 3: Innovative Defect Based Test Approaches (Session Chair: Joan Figueras, UPC, Spain)

2:30 - 2:50 Benoit Nadeau-Dostie, Mahiuzzaman Mahmud, Jean-François Côté and Fadi Maamari, "***Structural test with functional characteristics***"

2:50 - 3:10 Hans Manhaeve, "***Current Testing for Nanotechnologies: A Demystifying Application Perspective***"

3:10 - 3:30 Irith Pomeranz, Srikanth Venkataraman and Sudhakar M. Reddy , "***Fault Diagnosis and Fault Model Aliasing***"

3:30 - 3:45 Short Break

3:45 - 4:45 Session 4: IDDX Applications and Monitor Design - 2 (Session Chair: Mohammad Tehranipoor, UMBC, USA)

3:45 - 4:05 Anis Nazer, Ali Chehab, Ayman Kayssi and Rafic Makki, "***Evaluation of iDDT Testing for CMOS Domino Circuits***"

4:05 - 4:25 Surya Kumar, Scott Thomas, Rafic Makki, Ali Chehab and Ayman Kayssii, "***Simulation Modeling and Testing of SRAMs Using Dynamic Currents***"

4:25 - 4:45 Scott Thomas, "***An Introduction to Computer Algorithms Designed to Facilitate iDDT Current Testing of CMOS Circuits***"

4:45 - 5:00 Short Break

5:00 - 6:15:
Session 5: Panel: "Defect Based Testing in a Foundry Environment: Holy Grail or Reality?"

Coordinator: & Moderator:
Hank Walker, *Texas A&M University, USA*

Panelists:
Rob Daasch, *Portland State University*
Janusz Rajski, *Mentor Graphics Corp.*
R*ob Aitken, *ARM/Artisan

13th IEEE International Workshop on Current & Defect Based Testing

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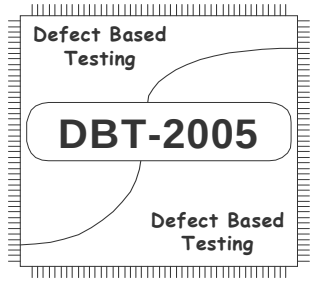

Napa Valley, CA

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PROGRAM INFORMATION

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IEEE Computer Society
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