DBT-2006 : IEEE INTERNATIONAL WORKSHOP on CURRENT & DEFECT BASED TESTING

October 26 - 27, 2006 ***Santa Clara Convention Center, Santa Clara, CA***

Held in conjunction with ***ITC Test Week (ITC-2006)***

CALL FOR PAPERS AND PARTICIPATION

Theme: *Defect-Based or Data-Based Testing: What's the difference?*

Defective parts are due to either systematic or random manufacturing defects. As new processes with new manufacturing steps evolve and new structures are meanwhile being developed, new defect mechanisms arise. To develop more appropriate fault models, a good understanding of, and a continuous follow-up on defect mechanisms -both systematic and random- is mandatory to support the manufacturability of today's and tomorrows integrated circuits, fuelling defect based test approaches. Increasing design complexity as well as the need to better cope with process variability shifts the focus from pass/fail oriented test to data-based test approaches, exploiting information on the neighborhood to support a better decision making. The requirement to distinguish between good and bad parts in a reliable way, taking into account the need to cope with process variability imposes a data-based defect-based test approach.

The IEEE International Workshop on **Current and Defect Based Testing (DBT 2006)** is aimed at addressing these issues and others related to **"Defect-Based or Data-Based Testing: What's the difference?"** Paper presentations on topics related to the workshop's theme and to those given below are expected to generate active discussion on the challenges that must be met to ensure high IC quality through the end of the decade.

- **Test Data Analysis**
- **Transition and Delay Testing**
- **I_{DDQ} and I_{DDT} Testing**
- **Low voltage Testing**
- **Noise and Cross-talk Testing**
- **Defect Coverage & Metrics**
- **Economics of Defect Based Testing**
- **Outlier Identification**
- **Data-Mining approaches for Test Data Processing**
- **Elevated Voltage Testing and Stress Testing**
- **Reliability and Yield**
- **Nanometer Test Challenges**
- **Mixed Current/Voltage Testing**
- **Fault Localization & Diagnosis**
- **Data-Based Testing**

To present at the workshop, submit a postscript or Acrobat (PDF) version of an extended abstract of at least 1000 words via E-mail to the **Program Chair** by Aug. 1, 2006. Each submission should include full name and address of each author, affiliation, telephone number, FAX and E-mail address. The presenter should also be identified. Camera-ready papers for inclusion in the digest of papers will be due on Oct. 6, 2006. Presentations on cutting edge test technology, innovative test ideas, and industrial practices and experience are welcome. Proposals for **Embedded Tutorials, Debates**, **Panel Discussions** or **"Spot-Light"** presentations describing industrial experiences are also invited.

AUTHOR'S SCHEDULE:

Submission of Extended Abstract:	**Aug 18, 2006**
Notification of Acceptance:	**Sep 15, 2006**
Camera Ready Paper:	**Oct 6, 2006**

Technical Program Submissions:
Mehdi Tahoori
Electrical & Computer Engineering
Northeastern University
Boston, MA 02115, USA
Tel: (617) 373-2032, x-8970(FAX)
E-mail: *mtahoori@ece.neu.edu*

General Information
Jim Plusquellic
Dept. of Electrical & Computer Eng.
University of Maryland, Baltimore County
Baltimore, MD 21250, USA
Tel: (410) 455-1349, x-3969(FAX)
E-mail: *Plusquel@csee.umbc.edu*

Visit our www site at: http://www.cs.colostate.edu/~malaiya/dbt.html

Sponsored by: **IEEE Computer Society Test Technology Technical Committee**