

ENHANCEMENT OF RESOLUTION IN SUPPLY CURRENT BASED TESTING FOR LARGE ICS

Yashwant K. Malaiya*
Computer Science Department
Colorado State University
Fort Collins CO 80523
(303) 491-7031
malaiya@cs.colostate.edu

Anura P. Jayasumana
Qiao Tong
Sankaran M. Menon
Electrical Engineering Department
Colorado State University
Fort Collins CO 80523

Abstract

Current drawn by a static CMOS VLSI integrated circuit during quiescent periods is extremely small and is normally of the order of nanoamperes. However, it is remarkably susceptible to a number of failure modes. Many faults present in such ICs cause the quiescent power-supply current (IDDQ) to increase by several orders of magnitude. Some of these faults may not manifest as logical faults, and would not be detected by traditional IC test techniques.

In large ICs, it may be hard to distinguish between larger IDDQ due to defects and elevated IDDQ due to normal parameter variations. A statistical characterization of the problem is presented. This can be used to determine the optimal size of partitions. A new information compression scheme is presented which can significantly enhance resolution.

1 INTRODUCTION

The use of leakage current measurement to detect faults in CMOS ICs has been under consideration for a number of years [1]. Recent studies on leakage current based testing techniques, [2], [3] have concluded that it is necessary to include IDDQ monitoring to obtain highly reliable CMOS ICs. The data presented for four sample CMOS ICs showed that the defect detection increased between 60% to 180% when IDDQ monitoring is added to a functional test set [2].

In the next section we review the research on current testing. In Section 3 we discuss the statistical characterization of the currents of the circuits. We analyze in Section 4 the partitioning of a circuit for the purpose of improving the resolution of the current testing. And in Section 5 we propose a new signature scheme for IDDQ testing. We conclude in Section 6.

*This work was partly supported by an SDIO/IST project monitored by ONR

2 BACKGROUND

There are several reasons for using IDDQ monitoring for testing of ICs [4], [5]. Traditional IC testing techniques are not effective in detecting a number of failure modes in CMOS ICs. In general, faults such as gate oxide shorts [4], [6]-[10], certain bridging faults [11]-[14], certain open faults, stuck-on faults [7], punch-through faults [15], parasitic devices, pn junction leakage, and abnormally high contact resistance, may not manifest as logic faults and therefore will not be detected by traditional tests which monitor the output logic levels. These localized defects degrade the electrical performance of the circuit without affecting the logical operation performed by the circuit. Parametric faults such as incorrect threshold voltage, excessive parasitics, etc., are also difficult to detect by traditional test techniques, and often affect circuit signal delays as well as the power consumption.

A major fraction of failures caused by circuit fatigue will first appear as parametric drifts. Progressive gate oxide leaks for example, may not initially affect the functionality of a device, but could become shorts during a short time leading to the failure of a device [7], [16]. Eventually some of them will advance enough to alter the logical behavior or circuit failure. Leakage current based testing will detect these parametric drifts before they actually change the circuit behavior. A wealth of data exists, that show that a device that fully passes the logic functional tests but fail the IDDQ test, fall in a significant category that functionally fail more frequently in early life than normal [4].

Current testing also is an invaluable tool for detecting faults in devices that contain both analog and digital functions on a single substrate [17]. By 1990 as much as 50% of the devices were expected to combine digital and analog functions on a single substrate [18].

The off-chip current testing has several other advantages over the traditional functional testing techniques [1]. In functional testing, the site of a fault has to be exited and

the effect of the fault has to be propagated to the output. In IDDQ testing, the propagation of the effect is automatic. Further, it can provide transistor level resolution as opposed to gate level resolution. Off chip current testing has proved to be very efficient for circuits like static RAMs [19].

Most of the gate oxide shorts cannot be modeled as stuck-at faults, especially for transistors with $W/L \gg 1$ [20]. The use of current measurement techniques to find the gate oxide leaks is investigated in [21], and techniques are presented to test quiescent IDDQ to a $1 \mu\text{a}$ limit on every clock phase of a functional test. It also identifies several problems associated with the measurement of IDDQ. The current drawn by I/O circuits for example, could mask the current drawn by a fault. Other problems identified include wideband noise across the load capacitance, dielectric absorption in output pads, input capacitance offered by the VDD pin, and the presence of mixed logic and redundant cells. To overcome these problems, they have proposed the use of several techniques during the design of ICs, including the use of separate VDD pins for output buffers and internal logic.

Stuck-on faults in CMOS circuits cannot be detected using traditional functional fault testing techniques. Test generation for detection of such faults, when IDDQ testing is used, is considered in [22]. Different decision processes involved in detecting such faults have been examined. It has been shown that IDDQ testing also detects multiple stuck-at faults as well as logically redundant faults [23].

Most of the research in this area considers the use of IDDQ measurement techniques for detection of faults in CMOS circuits. This can be attributed to the fact that the static quiescent current drawn by a CMOS circuit is very small and therefore the detection of a fault which increases the IDDQ is relatively easy to detect. With technologies such as NMOS and TTL, the quiescent current can be fairly large, and the increase in current drawn due to a fault may not be significant enough to be detected by measuring equipment. Even so, current testing techniques have been successfully used to detect faults in TTL circuits [24]. The faults that have been detected include open circuits, stuck at faults and multiple faults.

The supply current measurement has been supplemented in [25] with the measurement of low frequency noise in supply current, the circuit delay as a function of the supply voltage, transient current as the circuit switches between states, and the noise in transient current to provide indication of incipient failure of CMOS integrated circuits.

Several factors could complicate the testing of an IC by current measurements. One such example is the strong non-linear characteristics of certain defects. It has been suggested that IDDQ be measured at the highest possible VDD to overcome this problem. It has however been observed that a measurement of IDDQ vs VDD could often identify the nature of the defect causing IDDQ elevation [2]. High IDDQ logic states are inherent in some designs and may occur unintentionally in others. Examples of such conditions include internal bus contention states in microprocessors, and IC's with analog circuitry [26].

One obstacle for commercial acceptance of current test-

ing of ICs has been the relatively slow measurement rate compared to normal logic testing. Typically, current testing is done at a rate less than 100K test patterns per second [21], whereas the functional testing can be carried out at the normal operating frequency of the device under test. The speed of IDDQ testing is limited by several factors. The width of transient current pulse, loading of VDD pin due to output buffers and the impedance of the probing circuitry are some of them. It has been demonstrated that the rate of testing can be increased by several orders of magnitude by isolating the output buffers of an IC from the VDD pin [2].

The high resolution required for current testing has been sighted as another problem that makes current testing unacceptable at present [3].

The key to performing an effective IDDQ test is the probe circuit used to measure the current. Such a circuit should be capable of measuring small currents, without affecting the supply voltage especially during transients, and must be capable of fast measurements [27]. The different types of current probes in use are examined in [27], and a probe circuit has been proposed which allows a system to perform dynamic IDDQ tests as an integral part of the functional testing of a CMOS device.

Built-in current sensing techniques have been proposed to overcome the disadvantages of existing off-chip current testing techniques. Current sensors have been proposed and implemented using CMOS technology, some capable of detecting currents as small as $2\mu\text{a}$ at 1MHz clock frequency [3], [4]. In BIC testing, an IC is implemented using a number of modules and each module is connected to the power supply through a current sensor. The output of the current sensor of a module is observed with the proper input vectors to detect faults in that particular module. Test generation techniques have been proposed to detect several classes of faults using BIC sensing techniques.

The next section presents a statistical view of the resolution problem. It is next used for examination of the partitioning strategy. The fifth section presents a new signature scheme.

3 STATISTICAL CHARACTERIZATION

Some approaches suggested for current testing involve recording the entire waveform or recording the value of IDDQ once each cycle. These approaches involve recording and processing a large amount of information. They may not be suitable for testing a large volume of devices or for a built-in-test application. The best approach is to make a binary decision each time. The IDDQ value is compared with a previously decided threshold value. If the measured value exceeds the threshold, a fault is considered to have been detected. We assume this approach in the discussions below.

IDDQ based testing requires measurement of an analog

quantity rather than a digital signal in case of voltage testing. Both the normal and faulty values can vary significantly. To arrive at an upper limit of normal IDDQ and to examine limitations of IDDQ based testing, a statistical characterization of the problem is needed.

3.1 Resolution for Current Testing

In a normal CMOS device, one may view the overall conductance of the device (IDDQ/VDD) as the sum of conductances of individual cells, all connected in parallel (Fig. 1). If the supply voltage is assumed to be fixed, we can write

$$IDDQ = \sum_{j=1}^n i_{jDDQ} \quad (1)$$

where i_{jDDQ} is the quiescent supply current through cell j , and n is the total number of cells.

For each normal cell, i_{jDDQ} will vary depending on the parameter values as well as the input logic signals. It can therefore be regarded as a random variable, At this time not enough data exists that will enable us to find the applicable distribution. However for a first approximation using the central limit theorem [28], we can assume that IDDQ, being a summation, has a distribution which is approximately Gaussian. If the current through an average cell, i_A is characterized by μ_{iADDQ} and σ_{iADDQ} then we can assume,

$$\begin{aligned} \mu_{IDDQ} &= n \cdot \mu_{iADDQ} \\ \sigma_{IDDQ} &= \sqrt{n} \cdot \sigma_{iADDQ} \end{aligned} \quad (2)$$

Fig. 1. The parallel current paths in a CMOS device

Let us now assume that at most one leakage defect exists. This is not a limiting assumption as a multiple leakage

defect is likely to be tested more easily. Let us assume that the additional quiescent supply current, i_f , is characterized by the parameters μ_{if} and σ_{if} . Then the overall supply current in the presence of a defect is given by $IDDQ+i_f$ with the distribution given by

$$\mu_{IDDQf} = n\mu_{iADDQ} + \mu_{if} \sigma_{IDDQf} = \sqrt{n\sigma_{iADDQ}^2 + \sigma_{if}^2} \quad (3)$$

The distinction between the normal IDDQ and the faulty $IDDQ_f$ is easy if the two distributions are well separated. As most of the distribution is centered with $(\mu \pm 3\sigma)$, we can define the separation between the two distributions as (Fig. 2):

$$\begin{aligned} gap &= (\mu_{IDDQf} - 3\sigma_{IDDQf}) - (\mu_{IDDQ} + 3\sigma_{IDDQ}) \\ &= \mu_{if} - 3(\sqrt{n\sigma_{iADDQ}^2 + \sigma_{if}^2} + \sqrt{n} \cdot \sigma_{iADDQ}) \end{aligned} \quad (4)$$

Fig. 2. The 'gap' between normal and faulty values

This expression illustrates the basic problem in testing large devices. As n increases, the spread of the distributions also increase. For devices that are sufficiently large, the gap will become negative, i.e. the two distributions will overlap.

3.2 Deciding the threshold value

As we have discussed above, the most convenient setup for current monitoring compares the measured IDDQ with a preselected $IDDQ_{th}$. If the measured value is higher, the device is regarded to be faulty.

As discussed above, for larger devices, the distinction between the normal and faulty values may be hard to make. A more strict screening will use a lower value of $IDDQ_{th}$. However, this will result in a larger number of good devices being rejected.

Below we obtain an expression for the probability of incorrectly rejecting a good device.

Let $IDDQ_m$ be a measured value. Consider the following.

$$\begin{aligned} Prob \quad & \{ \text{device is good} \mid IDDQ_m > IDDQ_{th} \} \\ & = Prob\{IDDQ_m > IDDQ_{th} \mid \text{device is good}\} \end{aligned}$$

$$\begin{aligned}
& .Prob\{device\ is\ good\}/ \\
& [Prob\{I_{DDQm} > I_{DDQth} \mid device\ is\ good\} \\
& .Prob\{device\ is\ good\} \\
& + Prob\{I_{DDQm} > I_{DDQth} \mid device\ is\ bad\} \\
& .Prob\{device\ is\ bad\}] \tag{5}
\end{aligned}$$

where the RHS is obtained by using the Bayes' rule.

An optimal value of I_{DDQth} would be arrived at by considering the cost of rejecting a good device versus the cost of passing a bad device. Many devices are marginal, they allow a larger supply current, but the logical operation is correct. The cost of using these devices is the higher drain on the power source as well as significantly reduced reliability because of the heat generated.

4 PARTITIONING

From the discussion in the previous section, we have seen that the gap between the normal and faulty distributions will decrease when the number of cells n increases. If the number of the cells of a device exceeds a certain value, the gap becomes negative, i.e., the two distributions overlap. Under this situation, it would be difficult to distinguish the faulty current from the normal one. The solution to this problem will be to partition the device under test into modules. Each module will have its own current sensor. Thus these modules can be tested independently. Similar equations about the parameters of the distributions can be established for each module. And the size of each module can be controlled such that the faulty and normal distributions within each module can be distinguished.

Below we obtain the criteria for a valid partitioning for this device.

The same equation for the gap applies for each module:

$$gap = \mu_{if} - 3(\sqrt{n\sigma_{iADDQ}^2 + \sigma_{if}^2} + \sqrt{n}\sigma_{iADDQ}) \tag{6}$$

where n is the number of cells in one module.

Let us assume that maximum size of each module is determined by letting gap be 0. Although we have to use numerical method to obtain the exact value of n , we can derive the upper bound of n as follows:

$$\mu_{if} = 3(\sqrt{n\sigma_{iADDQ}^2 + \sigma_{if}^2} + \sqrt{n}\sigma_{iADDQ}) \geq 6\sqrt{n}\sigma_{iADDQ} \tag{7}$$

So the upper bound of maximum n , denoted by n_b , is

$$n_b = \left(\frac{\mu_{if}}{6\sigma_{iADDQ}}\right)^2 \tag{8}$$

Hence the device can be partitioned into modules whose sizes will not exceed n_b , and all the modules will have approximately the same number of cells.

There is another reason why we want to partition the device into several modules. The larger the device or circuit becomes, the larger the capacitance there will be at the current sensor input. So it will take longer period for

the current sensor to respond to show the value of the current flow in the circuit. The speed is limited due to the fact that the current monitoring has to be done after the transients have died down. The duration of the transients will depend among other things on the capacitance associated with measurement points. Thus the larger the circuit that is covered by a current monitor, the longer will be the transient time.

5 A NEW SIGNATURE SCHEME

Here a new scheme is presented, which reduces the probability of making an incorrect decision. It also allows for high IDDQ states, which may occur in some normal devices for some test vectors [21].

Consider application of a set of test vectors for which current monitoring is done. The output of the sensing circuit is a binary sequence where a '1' represents the fact that I_{DDQm} is greater than I_{DDQth} for that vector. Rather than basing a decision on a single '1', the string can be compressed into a signature, which can be used for evaluation. Since the faults cause a unidirectional error (i.e. 0 to 1) adding the number of '1's can be an appropriate signature. If this signature S is greater than a preselected value S_{th} , the device is rejected.

The effectiveness of this scheme is because of the fact that by multiple samplings, more information is used for decision making.

Consider a situation when m randomly chosen vectors are applied, where $m > S_{th}$. The probability of rejecting a good device then is given by the following:

$$\begin{aligned}
& Prob\{S > S_{th} \mid device\ is\ good\} \\
& = \sum_{S=S_{th}-1}^m \binom{m}{s} (1-p)^s p^{m-s} \tag{9}
\end{aligned}$$

where

$$p = Prob\{I_{DDQm} < I_{DDQth} \mid device\ is\ good\} \tag{10}$$

It is easy to see that this probability declines with increasing S_{th} . Let us also consider the probability of incorrectly accepting a bad device,

$$\begin{aligned}
& Prob\{S < S_{th} \mid device\ is\ bad\} \\
& = \sum_{S=0}^{S_{th}} \binom{m}{s} (1-q)^s q^{m-s} \tag{11}
\end{aligned}$$

where

$$q = Prob\{I_{DDQm} < I_{DDQth} \mid device\ is\ bad\} \tag{12}$$

Again it is easy to see that this probability increases with increasing S_{th} .

Thus the optimal value of S_{th} can be obtained only by obtaining a suitable cost function involving these two probabilities.

The simplest current sensor can be built with either a resistive or a capacitive element (labeled by 'X' in Fig. 3) along with a voltage comparator, as shown in Fig. 3. The current flow will cause a voltage drop on the element X and the voltage on X is fed to the comparator [27], [29]. The other input of the comparator is the standard voltage which would result from $I_{DDQ_{th}}$ on the same capacitor. Therefore, if the measured current I_{DDQ} is greater than $I_{DDQ_{th}}$, the output of the current sensor is 1. If I_{DDQ} is equal to or smaller than $I_{DDQ_{th}}$, the output of the current sensor is 0.

Fig. 3. A General Current Sensor

The signature is obtained by counting the number of times when the detected current flow exceeds $I_{DDQ_{th}}$, which is denoted by S . If $S \geq S_{th}$, as discussed in the previous paragraph, then the device is regarded to be faulty. The logic circuit that is used to extract the information about the signature is called signature extractor.

Since each module or subcircuit has its own current sensor, it is impractical to observe the output of every current sensor. One solution to this problem is to propagate the outputs of all the sensors to one observable output pin which is designed solely for the signature extractor. This signature extractor maybe implemented simply by an OR gate. The outputs from all the current sensors are fed to the OR gate. A counter is connected to the output of the OR gate, as shown in Fig. 4, to calculate the total number of times that the detected current I_{DDQ} exceeds $I_{DDQ_{th}}$, which is

nothing but the signature S .

Fig. 4. Partitioning and Information Compression

This signature extractor also works correctly if there are more than one faulty module since in that case S will be even greater than that when there is only one faulty module.

6 CONCLUSIONS

The statistical characterization of the quiescent current of a circuit module under normal and faulty conditions was first analyzed. The result was used to provide the criterion for partitioning a large circuit into smaller modules for higher resolution in current monitoring. Also a new signature scheme was proposed for IDDQ testing.

References

- [1] Y.K. Malaiya and S. Y. H. Su, "A new fault model and testing technique for CMOS devices," *Proc. Int. Test Conf.*, 1982.
- [2] C.F. Hawkins, J. M. Soden, R.R. Fritzscheier and L. K. Horning, "Quiescent power supply current measurement for CMOS IC defect detection," to appear in *IEEE Trans. Industrial Electronics*, May 1989.
- [3] W. Malay et.al., "Built in Current Testing," *Research Report No. CMUCAD-88-27*, Carnegie Mellon University.
- [4] K. Baker and B. Verhelst, "IDDQ testing because 'Zero Defects isn't Enough: A Philips Perspective,'" *Proc. IEEE Int. Test Conf.*, 1990.
- [5] S. McEuen, "Why IDDQ?," *Proc. IEEE Int. Test Conf.*, 1990.
- [6] C. R. Barrett and R. C. Smith, "Failure Modes and Reliability of Dynamic RAMs," *Proc. Int. Electron Devices Conf. (IEDM)*, Dec. 1976.

- [7] C. F. Hawkins and J. M. Soden, "Reliability and Electrical Properties of Gate Oxide Shorts in CMOS ICs," *Proc. IEEE Int. Test Conf.*, 1986.
- [8] S. Holland, I. Chen, T. Ma and C. Hu, "On Physical Models for Gate Oxide Breakdown," *IEEE Electron Dev. Ltr.*, vol EDL-5, No. 8, Aug. 1984.
- [9] C. Hu, "Thin Oxide Reliability," *Int. Electron Devices Conf. (IEDM)*, Dec. 1985.
- [10] J. M. Soden and C. F. Hawkins, "Electrical properties and detection methods for CMOS IC defects," *Proc. 1st European Test Conf.*, Apr. 1989.
- [11] J. M. Acken, "Testing for Bridging Faults (Shorts) in CMOS Circuits," *Proc. IEEE/ACM Design Automation Conf.*, June 1983.
- [12] F.J. Ferguson, M. Taylor, T. Larrabee, "Testing for Parametric Faults in Static CMOS Circuits," *Proc. IEEE Int. Test Conf.*, 1990.
- [13] Y. K. Malaiya, A. P. Jayasumana and R. Rajsuman, "A Detailed Examination of Bridging Faults," *Proc. IEEE Int. Conf. on Computer Design*, 1986.
- [14] S. D. Millman and E. J. McCluskey, "Detecting Bridging Faults with Stuck at Test Sets," *Proc. IEEE Int. Test Conf.*, 1988.
- [15] P. Richman, *MOS Field Effect Transistors and Integrated Circuits*, John Wiley, 1973.
- [16] C. F. Hawkins and J. M. Soden, "Electrical Characteristics and Testing Considerations for Gate Oxide Shorts in CMOS IC's," *Proc. IEEE Int. Test Conf.*, 1985.
- [17] J.F. Frenzel and P.N. Marinos, "Power supply current signature analysis: A new approach to system testing," *Proc. Int. Test Conf.*, 1987.
- [18] A. Santoni, "Mixed-Signal Devices Create Testing Headaches," *Electronic Test*, Feb. 1987
- [19] R. Meershoek, B. Verhelst, R. McInerney and L. Thijssen, "Functional IDDQ Testing on a Static RAM," *Proc. IEEE Int. Test Conf.*, 1990.
- [20] M. Syrzycki, "Modeling of gate oxide shorts in MOS transistors," *Res. Rep. CMU CAD-88-22*, Carnegie Mellon University, Apr. 1988.
- [21] C. Crapuchettes, "Testing CMOS IDD on large devices," *Proc. Int. Test Conf.*, 1987.
- [22] Y. K. Malaiya, "Testing stuck-on faults in CMOS integrated circuits," *Proc. Int. Conf. on Computer Aided Design*, 1984.
- [23] R.R. Fritzmeier, J.M. Soden and R.K. Treece, "Increased CMOS IC Stuck-at Fault Coverage with Reduced IDDQ Test Set," *Proc. Int. Test Conf.*, 1990.
- [24] M. Hashizume, K. Yamada, T. Tamesada and M. Kawakami, "Fault detection of combinational circuits based on supply current," *Proc. Int. Test Conf.*, 1988.
- [25] A.P. Dorey, B. K. Jones, A. M. Richardson, P. C. Russell and Y. Z. Xu, "Reliability testing by precise electrical measurement," *Proc. Int. Test Conf.*, 1988.
- [26] L.K. Horning, J. M. Soden, R. R. Fritzmeier and C.F. Hawkins, "Measurement of Quiescent Power Supply Current for CMOS ICs in production testing," *Proc. Int. Test Conf.*, 1987.
- [27] M. Keating and D. Meyer, "A new approach to dynamic IDD testing," *Proc. Int. Test Conf.*, 1987.
- [28] E. Parzen, *Modern Probability Theory and Its Applications*, Wiley, 1960.
- [29] A. Rubio, J. Figueras and J. Segura, "Quiescent Current Sensor Circuits in Digital VLSI CMOS Testing," *Electronics Letters*, July 1990.