ON ACCURACY OF SWITCH-LEVEL MODELING OF BRIDGING FAULTS IN COMPLEX GATES

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ABSTRACT

Bridging faults have been shown to be a major failure mode in VLSI devices. This study examines nMOS and CMOS complex gates in detail for bridging faults. Analysis is carried out using both switch and circuit level models for comparison. It is shown that in most cases, the switch level analysis predicts the correct behavior. A set of conditions are presented, under which the switch level analysis may fail to predict the correct behavior. These conditions can be used for accurate switch level test generation and simulation.

1. INTRODUCTION

In the past test generation and simulation has been done exclusively at gate level. In recent years, it has been pointed out that specially for MOS devices, the classical stuck at fault model does not represent some important failure modes. In a complex gate, the physical nodes do not directly correspond to nodes in an equivalent gate level network [1, 2]. Hence many physical opens and shorts cannot be satisfactorily represented at the gate level. Gate level model of faults in even simple gates in nMOS and CMOS can become quite complex [3-5]. Other options are to consider failure modes at switch level and circuit level. Circuit level simulators such as SPICE, can be used for the study of failure modes. However, with the increasing complexity of integrated circuits, use of circuit level simulators become impracticable even for moderate sized devices, due to very large CPU time requirement. As a consequence, switch level modeling has received more attention recently [3, 6-8]. A number of researchers have studied faults in complex gates [9-13]. This paper presents a comparative study of switch and circuit level modeling of CMOS and nMOS complex gates for bridging faults. Results reported here include a set of conditions under which the switch level analysis may fail in modeling bridging faults in complex gates, and therefore it becomes necessary to use a lower level of modeling.

MOS complex gates can be used to realize complex logic functions. An nMOS complex gate consists of one load transistor and a driver part which realizes the required function. The AND operation is obtained by connecting FETs in series, and the OR operation by connecting them in parallel. A CMOS complex gate in general, has an nMOS pull down part with a complementary pMOS pull up part. In steady state, only one part, either nMOS or pMOS, conducts. In switch level modeling each transistor is considered as a switch which takes one of the two possible states - open or closed. An open switch means that the transistor is not conducting, while a closed switch means that it is conducting, offering a very low resistance path. OFF resistance of a MOSFET is considered to be very high in comparison to its ON resistance.

In MOS circuits, the bulk (well) connection does not play a major role under normal operating conditions. In majority of digital ICs made on silicon substrate, the bulk of a nMOS transistor is connected to ground or the maximum negative voltage on chip. Similarly the bulk of a pMOS transistor is connected to Vdd or the maximum positive voltage. This ensures that the bulk - drain and bulk - source junctions never become forward biased. Thus the bulk (or well) becomes completely isolated and the possibility of a current through the bulk is eliminated. In this case, drain and source regions are interchangeable (except in situations like lightly doped drain or LDD type structures). Hence the device acts as a bidirectional switch controlled by the gate voltage. For example, when the gate voltage of a nMOS transistor is high, there will be a current flow from drain to source, drain being the node with higher voltage. When the gate voltage becomes low, the transistor offers a high impedance between source and drain. This is the basis for switch level model of MOS transistors.

In some IC designs the bulk (well) of a transistor is connected to its source node (rather than the maximum positive or negative voltages). This is generally true in silicon on insulator (SOI) technology [14-16] and some times in the common bulk silicon technology. Since under normal operation of a device, the source voltage of nMOS (pMOS) is lower (higher) than the drain voltage, there is no possibility of the bulk - drain junction becoming forward biased. In general the source-bulk connection results in lower body-effect, equal potential distribution, and may even result in less area. However, when the bulk of a transistor is connected to its source, its behavior can no longer be characterized as a bidirectional switch in all situations.

i. Consider the case when drain voltage Vd is greater than the source voltage Vs. When gate voltage is high the transistor conducts and provides a low impedance path between drain and source. When gate voltage is low transistor offers a high impedance between source and drain. The switch level model is valid for this case.

ii. When Vd $<$ Vs, the bulk - drain junction become forward biased. This provides a low resistance source to drain path through the bulk. The current through the transistor is no longer controlled by the gate voltage. Therefore, the MOSFET cannot be modeled as a switch controlled by the gate. In this case, the current through the device can cause significant power dissipation, which could even result in permanent failure of the device. This situation never occurs under normal operation of the device. However, as shown in later sections, this situation could arise in the presence of bridging faults.

Bridging faults can be divided into three classes [3]: (1) Bridging within a logic element, (2) Bridging between logical nodes without feedback, and (3) Bridging between logical nodes with feedback. This study mainly concentrates on bridging faults within a MOS complex gate. However, some of our results are related to bridging faults between logical nodes with/without feedback.

Bridging faults in nMOS and CMOS complex gates are examined under both bulk connection schemes ; (i) when the bulk is connected to the maximum negative or positive potential and (ii) when

the bulk is connected to the source. Validity of switch level modeling is examined under the single fault assumption. Only irredundant gates are considered in this paper. Our results are given in different sections according to the design and technology used for complex gates. For switch level analysis the following assumptions are used.

1. A transistor is an ideal switch. For an N-channel (P-channel) transistor a H (i.e. definitely recognized high voltage level) at the gate causes it to represent zero (infinite) resistance and a L causes it to represent infinite (zero) resistance. When the input is not definitely H or L (i.e. indeterminate), the transistor presents an indeterminate resistance.
2. The resistance of the load transistor in an nMOS gate is much higher than zero, but much less than infinity.
3. A node connected to both Vdd and ground only through infinite resistance paths will retain its previous voltage level (at least for a limited time). A node connected to both Vdd and ground through zero resistance paths will have an indeterminate voltage level.

It is sometimes possible to resolve an indeterminate situation by assuming a specific resistance ratio for P and N channel transistors. However this makes the model more complex. It can be shown that the resistance depends not only on the transistor dimensions, but also the position of the transistor in a network [21].

Some useful terms for this discussion are defined below. All the definitions are illustrated in Fig. 1.

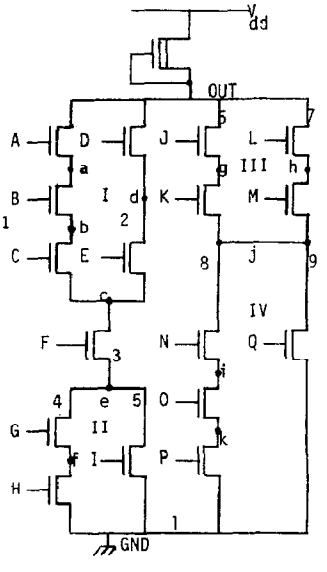

Fig. 1: Illustration of definitions.

Internal node of a gate : A node in a gate which is neither a transistor input (gate connection) nor the power supply is defined as an internal node. In Fig. 1, internal nodes are marked with lower case letters (a to l).

Column : A set of serially connected MOSFETs makes a column. In a column there are no transistors (or sets of transistors) in parallel. In Fig. 1, nine columns are shown, marked 1 to 9.

Parallel connected columns (PCC): A structure with more than one column in parallel. Fig. 1 has four PCCs, marked I to IV.

Internal node of a PCC : Any node in a PCC which is not common to another PCC is defined as an internal node of the PCC. In Fig. 1, nodes a, b and d are internal nodes of PCC I, f is an internal node of PCC II, g and h are internal nodes of PCC III, and i, j and k are internal nodes of PCC IV.

Conduction path : Any path which connects ground and output node will be called a conduction path. Fig. 1 has following conduction paths - ABCFGH, ABCFI, DEFI, DEFGH, JKNOP, JKQ, LMNOP and LMQ.

Logical node: A logical node is a logical input or an output node of a gate or a complex gate. In general all logical nodes are outputs of gates or complex gates.

Deterministically Testable Fault: A fault is deterministically testable if there is at least one vector which will definitely (under the switch level modeling assumptions) cause the logical output to be the complement of the output of fault free circuit.

In the next section we consider switch level modeling of nMOS complex gates with different bulk connections. In Section III CMOS complex gates are considered.

2. NMOS COMPLEX GATES

In this section the behavior of nMOS complex gates is examined. All possible bridging faults in a gate are considered, under single fault assumption.

A complex gate in nMOS technology is shown in Fig. 2, with all the possible shorts. Each fault has been investigated under all possible test vectors at switch level as well as at circuit level (using SPICE).

It is observed that all faults are deterministically testable. there is at least one vector which will definitely detect the fault. When the faulty output is indeterminate under our switch level analysis assumptions, the fault is not considered to be deterministically testable. For all of the faults, the switch level analysis is found to be in perfect agreement with circuit level analysis. This includes the cases when the indeterminacy of the switch level analysis is resolved at the circuit level because of specific circuit level parameters used. When the switch level analysis results in an indeterminate value, the circuit level analysis can often predict a definite logic value. This is not necessarily an advantage because with different parameters, the circuit level analysis can yield a different value.

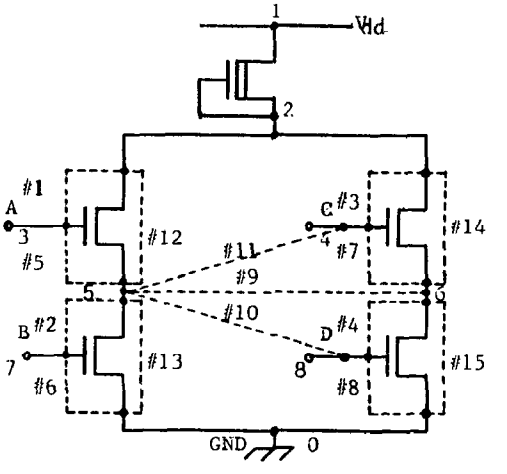

Fig 2: nMOS complex gate for example 1.

The complex gate shown in Fig. 3 is the dual of Fig. 2. It has also been examined for all possible shorts under all test vectors at both switch and circuit level. It is observed that (i) switch level analysis is in perfect agreement with circuit level analysis and, (ii) all the faults are deterministically testable. From the above study we can obtain some very useful results. Some important results, which are applicable when bulk is connected to ground are given below.

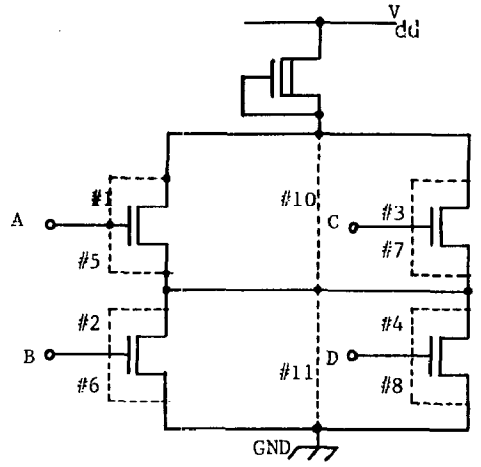

Fig. 3: nMOS complex gate, dual of Fig. 1.

2.1 NMOS COMPLEX GATES: BULK CONNECTED TO GROUND

Lemma 1: In an nMOS gate any short between two logical nodes will result in AND bridging between the affected inputs.

Proof : Two types of situations are possible - (i) Both inputs have same logic value, (ii) Inputs have different logic values. When both inputs have same logic value, short will be of no consequence. In the case when inputs have different value, the resultant logic value can be obtained as follows : Let us consider the resistance of pull-up transistor be r_H and ON resistance of nMOS in driver part be r_L. As r_H is a few orders of magnitude greater than r_L [3, 22], a hard short would always cause both nodes to be in low logic range. Thus the hard short will result in AND bridging. This can be seen clearly with Fig. 4. In case of bridging, both inputs i_A and i_B will appear as '0', if any one of them is '0'. QED.

Lemma 1 is also applicable to the case when the shorted nodes are inputs to a single gate or complex gate.

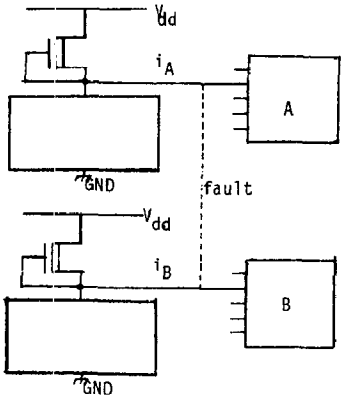

Fig. 4: Illustration for Lemma 1.

Theorem 1 : Output behavior of an nMOS gate, in the presence of a bridging fault (short) can always be correctly modeled at switch level.

A MOS transistor behaves like a bidirectional switch when bulk is connected to ground. Thus a short between two nodes does not violate any assumption of switch level model. Hence the logical behavior of the gate can always be correctly predicted at switch level.

Theorem 2 : In an nMOS gate, if a bridging fault occurs between any two nodes then there exists at least one vector for which logic output is different from that of the fault free gate.

Proof : This theorem is applicable only to the testable faults. Faults like bridging between two inputs of a NAND gate are not testable and theorem does not apply. To prove this theorem we will consider all possible conditions separately.

(i) When a fault occurs between two logical inputs: from lemma 1, short will result in AND bridging. Thus a faulty input '1' will appear as '0' if another faulty input is '0'. Hence the transistor will remain OFF, although correct input was '1'. Thus the output will be different from normal.

(ii) When the fault is between one input and one internal node of a gate : if the internal node is ground, then input will appear as s-at-0 and hence the transistor will appear s-OFF. If power supply and ground are shorted then the gate will appear as s-at-0. If power supply and the output node are shorted, then the gate will appear as s-at-1. If one input and the output node are shorted then gate will appear as s-at-0 for faulty '0' input. If an input is shorted with an internal node of a PCC, the gate will appear as s-at-0 when the faulty input is 0 and the inputs to the transistors between output and the faulty internal node are held at 1. This situation is shown in Fig. 5a. All the transistors between output and faulty internal node (f3) will conduct when their inputs are held high. If power supply is shorted with an internal node of a PCC, then with '1' at the inputs to the transistors between ground and faulty internal node, gate will appear as s-at-0.

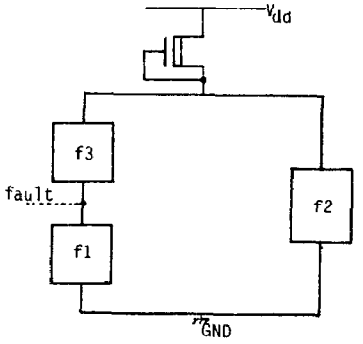

Fig. 5a: Illustration for Theorem 2.

(iii) When the short occurs between two internal nodes : if both nodes belong to one conduction path, all transistors between faulty nodes will appear as s-ON and their inputs become don't care terms. If the short occurs between two internal nodes of two different conduction paths, then the gate will perform one product of sum operation in place of sum of product. This situation is shown in Fig. 5b. The faulty output becomes (f1+f3)(f2+f4) in place of (f1f2 + f3f4). QED.

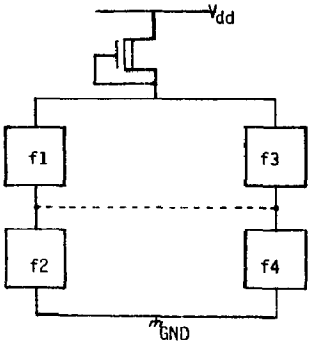

Fig. 5b: Illustration for Theorem 2.

2.2 NMOS COMPLEX GATES : BULK CONNECTED TO SOURCE

In this section we will discuss the behavior of nMOS gates under different bridging faults for the case when the bulk of a transistor is connected to its source.

We use the structures of Fig. 2 and Fig. 3 as examples again. Each fault has been investigated under all possible test vectors at switch level as well as at circuit level (using SPICE). Results are shown in Tables I and II. When the value predicted by SPICE is outside of the noise margins, it is termed probably high or probably low, depending on which side of the switching threshold it is on. It can be seen that all the faults are deterministically testable. For most of the faults, switch level analysis is found to be in agreement with circuit level analysis.

NC	NB	ND	NA	Normal	1	2	5	6	9	10	11	12	13
0	0	0	0	1	0,0	1,1	1,1	1,1	1,1	1,1	1,1	1,1	1,1
0	0	0	1	1	1,1	0,0	1,1	1,1	1,1	0,0	1,1	1,1	0,0
0	0	1	0	1	0,0	1,1	1,1	1,1	1,1	1,1	1,1	1,1	1,1
0	0	1	1	1	1,1	0,0	1,1	1,1	1,1	0,0	1,1	1,1	0,0
0	1	0	0	1	0,0	1,1	1,1	1,1	1,1	1,1	1,1	0,0	1,1
0	1	0	1	0	1,1*	1,1*	1,1	1,1	0,0	0,0	0,0	0,0	0,0
0	1	1	0	1	0,0	1,1	1,1	1,1	0,0	1,1	1,1	0,0	1,1
0	1	1	1	0	1,1*	1,1*	1,1	1,1	0,0	0,0	0,0	0,0	0,0
1	0	0	0	1	0,0	1,1	1,1	1,1	1,1	1,1	1,1	1,1	1,1
1	0	0	1	1	1,1	0,0	1,1	1,1	0,0	1,1	0,0	1,1	0,0
1	0	1	0	0	0,0	0,0	0,0	0,0	0,0	0,1*	0,1*	0,0	0,0
1	0	1	1	0	0,0*	0,0	0,0	0,0	0,0	0,0*	1,1*	0,0	0,0
1	1	0	0	1	0,0	1,1	1,1	1,1	1,1	1,1	1,1	0,0	1,1
1	1	0	1	0	1,1*	1,1*	1,1	1,1	0,0	0,0	0,0	0,0	0,0
1	1	1	0	0	0,0	0,0	0,0	0,0	0,0	1,1	1,1	0,0	0,0
1	1	1	1	0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	0,0

1* : Probable H (3.4-2.5 volts)
0* : Probable L (2.5-1.5 volts)
x,y : results of switch level and circuit level analysis respectively.

Table I: Analyses for nMOS complex gate in Fig. 2 (bulk connected to source).

ND	NC	NB	NA	Normal	1	2	5	6	13	14
0	0	0	0	1	0,0	1,1	1,1	1,1	1,1	1,1
0	0	0	1	1	1,1	0,0	1,1	1,1	1,1	0,0
0	0	1	0	1	0,0	1,1	1,1	1,1	0,0	1,1
0	0	1	1	0	1,1*	1,1*	1,1	1,1	0,0	0,0
0	1	0	0	1	0,0	1,1	1,1	1,1	0,0	1,1
0	1	0	1	0	1,1*	0,0	1,1	0,0	0,0	0,0
0	1	1	0	1	0,0	1,1	1,1	1,1	0,0	1,1
0	1	1	1	0	1,1*	0,0	1,1	0,0	0,0	0,0
1	0	0	0	1	0,0	0,0	0,0	1,1	1,1	0,0
1	0	0	1	1	1,1	0,0	1,1	1,1	1,1	0,0
1	0	1	0	0	0,0	1,1*	0,0	1,1	0,0	0,0
1	0	1	1	0	0,0	1,1*	0,0	1,1	0,0	0,0
1	1	0	0	0	0,0	0,0	0,0	0,0	0,0	0,0
1	1	0	1	0	0,0	0,0	0,0	0,0	0,0	0,0
1	1	1	0	0	0,0	0,0	0,0	0,0	0,0	0,0
1	1	1	1	0	0,0	0,0	0,0	0,0	0,0	0,0

1* : Probably H (2.7-2.2 volts)
0* : Probably L (2.2-1.25 volts)
x,y : results of switch level and circuit level analysis respectively

Table II: Analyses for nMOS complex gate shown in Fig. 3 (bulk connected to source).

However, there are some cases when switch level analysis does not match with circuit level analysis. For those situations a more detailed analysis below the switch level is essential. This is best illustrated by an example.

Example I - Let us consider the nMOS complex gate of Fig. 2 with fault #10 (short between node 5 and 8). Consider the test vector ABCD = 0011. The complex gate implements the function AB+CD. A simple switch level analysis suggests that the transistors NA and NB are OFF, and transistors NC and ND are ON. One end of the short, node 5, is between two OFF transistors. According to the assumptions of the switch level analysis, the presence of the short should be of no consequence. The output being connected to the ground through NC and ND both of which are ON, should be at logic 0.

However, SPICE analysis gives an output voltage of 2 volts, which is neither logic '0' nor '1'. SPICE outputs of faulty and fault free gate are shown in Fig. 6. The analysis also gives a current of about 20 μA, flowing from node 5 to 2. According to the switch level model, there should be no current through NA except for a small leakage current.

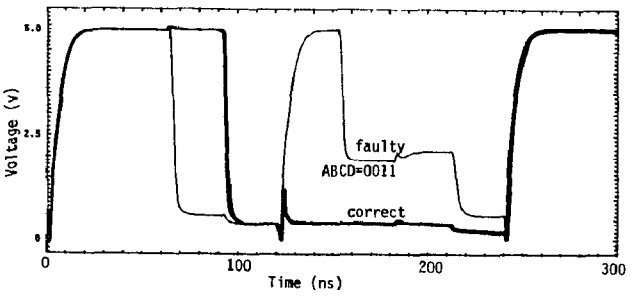

Fig. 6: SPICE output for example 1.

The circuit level analysis suggests that the resistance of the OFF transistor NA is not as close to the ideal (infinite) as the switch level analysis assumes. The significantly low OFF resistance and thus abnormally large leakage current through transistor NA can be explained as follows: In the normal operation, the channel current is controlled by the gate voltage and is almost independent of drain voltage. A depletion region devoid of mobile carriers is formed and therefore insulates the channel from rest of the substrate. No significant current passes through the substrate because the p-n junction between drain and bulk is reverse biased. In this present case, as voltage at node 8 and hence at node 5 is higher than the voltage at node 2, the p-n junction between bulk and drain is forward biased. Consequently a large leakage current flows through the bulk to the drain of transistor NA, making the OFF resistance considerably low. The phenomenon will be referred to as **Anomalous Reverse Conduction (ARC)**.

The effect of ARC can be seen in the equivalent circuit of a MOSFET shown in Fig. 7 [18]. In case of bulk source connection for Vs > Vd the, diode D1 becomes short circuited and diode D2 becomes forward biased.

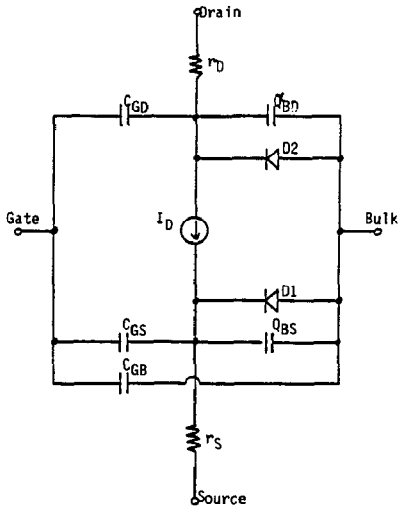

Fig. 7: SPICE model for MOSFET.

Example 1 is restricted to one PCC. When a bridging fault occurs between two nodes of two different PCCs, the situation becomes more complicated. In that situation it is possible that fault may become untestable at switch level. This is illustrated in example II

Example II - Consider the nMOS complex gate shown in Fig. 8, which implements the function (CD+E)(AB+F). Consider a bridging fault between nodes 4 and 6 and a test vector ABCDEF = 100010. Under these conditions, switch level analysis suggests that transistors ND, NC, NB and NF are OFF and transistors NA and NE are ON. As there is no direct connection between the output and the ground, output should be logic '1'. However, circuit level analysis (SPICE) gives the output voltage to be about 0.93V which is recognized as logic '0' by the subsequent stage. The SPICE analysis also gives a current flow from node 5 to 4, having a magnitude approximately 22 μA. According to switch level model there should not be any current (except for leakage) through transistor NC. *This contradiction between switch level analysis and circuit* level analysis again suggests that switch level analysis is not adequate for representing the circuit behavior.

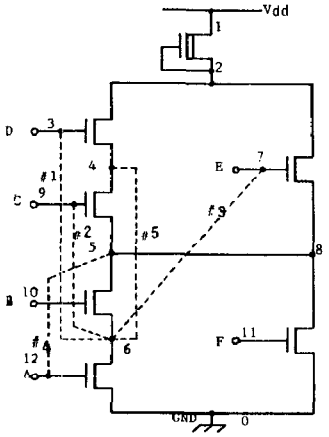

Fig. 8: nMOS complex gate for example 2.

The equivalent circuit of complex gate is shown in Fig. 9, which shows a path from output to ground. As node 4 is connected to ground with a low resistance path, and node 8 is connected to Vdd with a low resistance path, voltage at node 8 is higher than that at node 4. There will be a current flow from node 8 to 4 through NC, as a consequence of the ARC phenomenon.

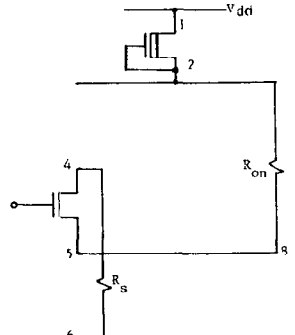

Fig. 9: Equvalent circuit of Fig. 9 under vector (100010).

Now consider some other bridging faults between two nodes of two PCCs. Using the same complex gate shown in Fig. 8, other faults are shown as 1,2,3 and 4. All these faults have the same nature as the fault discussed in Example I. It can be easily verified that under input vectors ABCDEF = 001101, 001101, 000111 and 110010 the switch level analysis predicts an output value of '0' for faults 1,2,3 and 4 respectively, while circuit level analysis (SPICE) suggests a value of logic '1'. These situations can be resolved by taking into account the ARC phenomenon. The above observations lead us to some very useful results which are applicable when the bulk is connected to the source of each transistor. Lemma 1, from the previous section is still applicable in this case. Theorems 1 and 2 are also applicable but only in special situations. They are restated below in a restricted form.

Lemma 2 : If source voltage of a nMOS transistor becomes higher than the drain voltage, then the behavior of that transistor cannot be modeled at switch level because of the anomalous reverse conduction (ARC).

Theorem 3: In an nMOS gate, for any short between two internal nodes of a PCC, the output behavior can be correctly modeled at switch level.

Proof: For ARC to occur, the drain of a transistor must be connected to ground and the source to V_{out} (which should be approximately equal to Vdd). For the drain to be connected to ground, there must be a low resistance path from the drain to the upper common node of the PCC, which should be connected to the ground through at least one of the parallel columns of the PCC. However, if the upper common node of the PCC is connected to ground, there can not be any internal node in the PCC with voltage higher than ground. There is then no way, the source of the transistor can be connected to V_{out} because of an internal short. QED.

Theorem 4: In an nMOS gate, if a short occurs between two internal nodes of a PCC, then there exist at least one vector for which the logic output is different from normal.

Proof of this theorem follows from Theorem 3 and the proof of Theorem 2 of section 2.1, for condition (iii).

Theorem 5 : In an nMOS gate if a short between two columns involve one non- logical node within a column and one logical node except ground, then there is at least one vector under which switch level analysis is not applicable.

Proof : Two situations are possible - (i) When both columns belong to one PCC and (ii) When columns belong to different PCCs. We will consider the two cases separately.

(i) When both columns belong to one PCC: Consider the case when one end of the fault is 1, i.e., it is the power supply or an input which can be set to 1. The transistor(s) will show ARC under the following conditions (a) All conduction paths are OFF except the one with the affected PCC. (b) All transistors of all healthy columns of affected PCC are OFF, and (c) All transistors in the column of faulty logic input are ON and all transistors in the column of nonlogic faulty node have gate voltage '0'.

(ii) When columns belong to different PCCs: The transistor(s) will show ARC when following conditions are met:- (a) All conduction paths are OFF except which have the affected PCCs. (b) All transistors of all healthy columns in the PCC of faulty logic input are OFF, while all transistors in the column of faulty logic input are ON, and (c) All transistors of the column of faulty nonlogic node are OFF, while all transistors in all healthy columns in same PCC are ON.

In both situations some transistor(s) will show ARC as their source potential become higher than the drain potential. Hence from Lemma 2, switch level model cannot be used to predict the behavior of these transistor(s). QED.

Theorem 6 : In an nMOS gate, for any short between two internal nodes of different PCCs, there exist at least one vector under which some transistor(s) show ARC, and hence switch level analysis is not applicable.

Proof : To prove this theorem we will consider all the possible situations separately

(1) When both PCC belong to one conduction path-let PCC1 and PCC2 be the PCC's involved in the fault which are closer to the output node and ground respectively. Some transistor(s) will show ARC when following conditions are met -

(a) All conduction paths are OFF except the one which has affected PCCs.

(b) In PCC1, all transistors in the faulty column have a '0' at their gates, while other columns are ON.

(c) In PCC 2 the transistors between faulty node and ground are switched ON, while all other transistors are switched OFF.

(2) When the two PCCs belong to different conduction paths, some transistor(s) will show ARC when following conditions are met -

(a) All conduction paths are OFF except the paths which have affected PCCs.

(b) All transistors in the faulty column of one PCC have a '0' at their gates, while all other columns are ON.

(c) All transistors in the other PCC have a '0' at their gates except the transistors between faulty node and output node.

In both the situations source potential of some transistor(s) become higher than the drain potential, hence they will show ARC. Therefore, from lemma 2 switch level model is not able to predict the behavior of these transistor(s). QED.

3. CMOS COMPLEX GATES

In CMOS technology, like in nMOS technology designs exists where (i) bulk is connected to ground (for nMOS) or power supply (for pMOS), or (ii) bulk is connected to source. For both cases, CMOS complex gates shown in Fig.2 and Fig.3 have been investigated under all possible shorts, for all test vectors at switch and circuit level (see Fig. 10 and Fig. 11). The results for design (i) are given in Tables III and IV. It has been observed that

(i) switch level analysis is in agreement with circuit level analysis
(ii) majority of the faults are not deterministically testable.

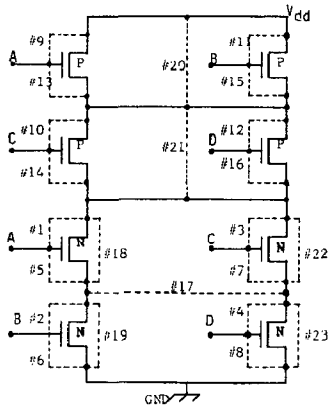

Fig. 10: CMOS complex gate corresponding to Fig. 2.

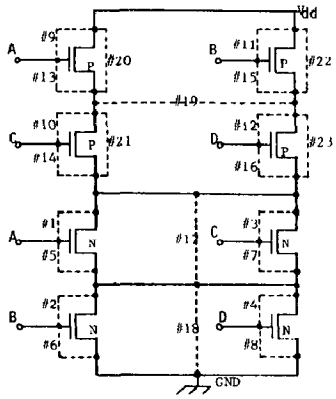

Fig. 11: CMOS complex gate corresponding to Fig. 3.

NA	NB	NC	ND	Normal	1	2	5	6	9	10	13	14	17	18	21	22
0	0	0	0	1	u,0*	1,1	1,1	1,1	1,1	1,1	1,1	1,1	1,1*	u,u	0,0*	1,1	1,1
0	0	0	1	1	u,0*	1,1	1,1	1,1	1,1	1,1	1,1	1,1	0,0	u,u	0,0	1,1	1,1
0	0	1	0	1	u,0	1,1	1,1	1,1	1,1	1,1	1,1	1,1	1,1	u,u	1,1	1,1	1,1
0	0	1	1	0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	u,0	1,1	0,0	u,1
0	1	0	0	1	u,0	1,1	1,1	1,1	u,0*	1,1	1,1	0,0	u,0*	u,0*	u,0*	1,1	1,1
0	1	0	1	1	u,0	1,1	1,1	1,1	u,0*	1,1	1,1	0,0	1,1	u,0*	u,0*	1,1	1,1
0	1	1	0	1	u,0	1,1	1,1	1,1	u,0*	1,1	u,0*	0,0	1,1	u,0*	1,1	1,1	1,1
0	1	1	1	0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	u,1	0,0	u,1*	
1	0	0	0	1	1,1	u,1*	1,1	1,1	1,1	u,0*	1,1	1,1	u,1	1,1	u,0*	1,1	1,1
1	0	0	1	1	1,1	u,u	1,1	1,1	1,1	0,0	u,1*	1,1	0,0	1,1	u,0*	1,1	1,1
1	0	1	0	1	1,1	u,u	1,1	1,1	1,1	0,0	1,1	1,1	1,1	1,1	1,1	1,1	1,1
1	0	1	1	0	u,u	0,0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	u,1	0,0	u,1*
1	1	0	0	0	u,1*	1,1	1,1	1,1	0,0	0,0	0,0	0,0	0,0	u,1*	0,0	u,1	0,0
1	1	0	1	0	u,1*	u,1	1,1	1,1	0,0	0,0	0,0	0,0	0,0	u,u	0,0	u,1*	0,0
1	1	1	0	0	u,1*	u,u	1,1	1,1	0,0	0,0	0,0	0,0	u,0*	u,u	u,1*	u,1*	0,0
1	1	1	1	0	u,u	u,0*	0,0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	u,u	0,0	0,0

u : undefined
1* : Probably H (3.4-2.5 volts)
0* : Probably L (2.5-1.5 volts)
x,y : results of switch level and circuit level analysis respectively.

Table III: Analyses for CMOS complex gate of Fig. 10.

NA	NB	NC	ND	Normal	1	2	5	6	9	10	13	14	17	18	19	20	21
0	0	0	0	1	u,0*	1,1	1,1	1,1	1,1	1,1	1,1	1,1	u,1*	u,0*	1,1	1,1	1,1
0	0	0	1	1	u,0	1,1	1,1	1,1	u,0*	1,1	0,0	0,0	u,0*	u,0*	1,1	1,1	1,1
0	0	1	0	1	u,0	u,0*	u,u	1,1	1,1	u,0*	1,1	1,1	1,1	1,1	1,1	1,1	1,1
0	0	1	1	0	u,0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	u,1*	0,0	u,1*	0,0
0	1	0	0	1	u,0	1,1	1,1	1,1	u,0*	1,1	0,0	0,0	u,0*	u,0*	1,1	1,1	1,1
0	1	0	1	1	u,0	1,1	1,1	1,1	0,0	1,1	0,0	0,0	u,0*	u,0*	1,1	1,1	1,1
0	1	1	0	0	u,0	u,1*	1,1	1,1	0,0	0,0	0,0	0,0	0,0	u,1*	0,0	u,1*	u,0
0	1	1	1	0	0,0	u,0*	0,0	0,0	0,0	0,0	0,0	0,0	0,0	u,1*	0,0	u,1*	0,0
1	0	0	0	1	1,1	u,0*	1,1	1,1	1,1	0,0	1,1	u,1*	1,1	u,0*	1,1	1,1	1,1
1	0	0	1	0	u,1*	0,0	1,1	0,0	0,0	0,0	0,0	0,0	u,u	0,0	u,1*	u,0	u,0*
1	0	1	0	1	1,1	u,0*	1,1	1,1	1,1	0,0	1,1	1,1	1,1	1,1	1,1	1,1	1,1
1	0	1	1	0	u,u	0,0	u,0*	0,0	0,0	0,0	0,0	0,0	0,0	u,1*	0,0	0,0	0,0
1	1	0	0	0	u,1*	1,1	u,1	1,1	0,0	0,0	0,0	0,0	u,u	0,0	u,1*	0,0	0,0
1	1	0	1	0	u,1*	u,0*	u,1	0,0	0,0	0,0	0,0	0,0	u,u	0,0	u,1*	0,0	0,0
1	1	1	0	0	u,1*	u,1*	u,0*	1,1	0,0	0,0	0,0	0,0	0,0	u,1*	0,0	0,0	0,0
1	1	1	1	0	u,1*	u,0*	0,0	0,0	0,0	0,0	0,0	0,0	0,0	u,0*	0,0	0,0	0,0

Table IV: Analyses for CMOS complex gate of Fig. 11.

The reasons of difficulties in testing CMOS bridging faults have been presented by Malaiya et al. [3,7].

It should be noted that the faults between internal nodes of n-part and p-part have not been examined as the likelihood of these faults is very small. From this study of CMOS gates we observed some very important results which are applicable to both designs.

Theorem 7 : In an irredundant CMOS complex gate, if two nodes within n-part or within p-part are bridged, then there exists at least one vector under which both n-part and p-part are either ON or OFF, provided that ARC does not occur.

Proof : From Theorem 2, any short between two nodes within n-part will change the operation of n-part. Similar arguments are applicable to p-part. In normal operation only one part either p or n gets ON, while other remain OFF. Because of the complementary nature, if operation of one part changes due to the fault then both parts will perform the same operation, i.e. both will be either ON or OFF. QED.

In fault detection procedure of CMOS combinational logic circuits, generally two pattern tests are used. The first pattern is applied to initialize the output and second pattern is used to detect the fault [19]. As Theorem 7 suggests, during certain faults both p-part and n-part may become OFF, and hence two pattern test procedures become necessary. Situations when both p-part and n-part become OFF are highly likely in the presence of a bridging fault between source and gate of a transistor, as this type of a bridging fault makes the transistor s-OFF. If such a fault occurs in n-part (p-part), then first test pattern should bring the output to logic '1' (logic '0'), while second test pattern should attempt to provide a low resistance path between output and ground (power supply) through the faulty transistor. It is possible that due to time skews or unequal delays along different paths of circuit, spurious logic values may occur during transition from first test pattern to second test pattern. These spurious logic values may result in failure of fault detection.

To illustrate this situation, let us consider fault #9 in the CMOS complex gate shown in Fig. 10. To initialize the output node to '0', first test pattern can be chosen out of seven possible vectors (1100, 1110, 1101, 0011, 1011, 0111, 1111). The second test pattern can be chosen out of three possible vectors (0100, 0110, 0101). Dur-

ing transition from first test pattern to second test pattern, it is possible that input vector take one state out of three possible states (x010, x001, x000), which can spuriously charge the output node. Because of this charging, output will appear at logic '1' during second test pattern. Therefore the test sequence will fail to detect the fault. Such situations for s-open faults has been reported in literature [20]. Ref. [20] gives two methods, by utilizing some additional transistors, to avoid these situations. When both P and N parts are ON, the fault is not deterministically testable by logic testing [22]. However, such faults may be detected using methods, which involve monitoring the supply current [22,23].

4. CONCLUSIONS

A careful study of several nMOS and CMOS complex gates has been done for all possible bridging faults. For most of the faults, in designs where the bulk is connected to ground, switch level analysis is found to be in agreement with circuit level analysis using SPICE. However, when the bulk is connected to source, there are some cases in which results from switch level analysis do not match with those from circuit level analysis. It has been demonstrated that all the faults within a PCC of an nMOS complex gate are deterministically testable by the vectors generated by switch level model. For faults like gate to source, gate to drain and drain to source shorts, the switch level model is adequate for obtaining the necessary test vectors. For shorts between a logical input and a nonlogical node of another column, switch level model does not correctly predict the behavior under all vectors in the case where bulk is connected to source. In these cases an analysis at a level below the switch level is essential. Also, when a short occurs between two nodes of two different cells, switch level model may not be accurate enough to generate necessary test vectors. Under some specific conditions the ARC phenomenon must be taken into account.

In a CMOS complex gate, a large fraction of faults are not deterministically testable, even though switch level analysis is found to be in agreement with circuit level analysis.

Switch level analysis can be used very effectively to characterize faults in nMOS and CMOS devices, with a reasonable amount of computations. But in some specific cases, the circuit level behavior must be taken into account for accuracy. Simple techniques for doing this without actually having to use detailed models such as that used in SPICE are considered elsewhere [17].

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