A NEW FAULT MODEL AND TESTING TECHNIQUE FOR CMOS DEVICES*

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Abstract

The CMOS (Complementary Metal Oxide Semiconductor) technology is expected to emerge as a very important technology for VLSI (very Large Scale Integration), because of several advantages it offers. Therefore, testing large CMOS networks has become very important.

A new fault model and a new testing technique are presented here. The leakage current (static supply current) which is normally very small, is very susceptible to some important physical failure modes in CMOS devices. In this paper, testing by measuring the leakage current under different input and state vectors is considered. Analysis of experimental data on some complex devices is reported.

Introduction

Some desirable properties of CMOS technology have been well known [1,2]: low static power dissipation, excellent noise immunity (typically 45% of the full logic swing), controlled rise and fall times and wider temperature and supply voltage ranges. Still in the past, bipolar and NMOS have been the dominant integrated circuit technologies. The situation has recently changed and CMOS has emerged as a contender for the leading position [3]. The CMOS costs are approaching NMOS costs. Power dissipation, a significant VLSI design problem, is expected to give CMOS an edge over NMOS [4]. It is estimated that in the 1985 semicustom market, CMOS will have a 32% share, about equal to the 36% bipolar share [5]. CMOS is also the most testable technology [6]. Therefore, testing of CMOS devices has assumed considerable significance.

The classical stuck-at fault model has so far been quite successful. It is simple to use and works well for a large fraction of physical failure modes [8]. Well-developed test generation methods are available which assume stuck-at faults. However, it has recently been pointed out that the stuck-at fault model does not represent some types of faults [10] (and sometimes non-existing faults are modeled [7]). This is especially true for MOS and CMOS [2,8,9,10]. A new fault-model is introduced here which supplements the stuck-at fault model.

The causes of physical failures in CMOS devices have been extensively studied [21]. Some of the significant physical failure mechanisms in CMOS are [11]:

- Open circuits, within a transistor or interconnection
- short circuits
- threshold dirft
- surface contamination

Ideally, when a CMOS integrated circuit is not switching, it should draw no supply current. Practically, a very small current (of the order of a few nanoampere), called leakage current, flows through the circuit. This current is very susceptible to some physical failures. Short circuits[23] (bridging faults) across transistors, threshold drift and surface contamination can all cause excessive leakage. Excessive leakage indicates either an existing logical fault or a marginally good device which is likely to fail early. A device with excessive leakage will be referred to as having a leakage fault. The process of testing circuits based on measuring the leakage current is called leakage testing.

A report [8] indicates the following possible failure modes causing logical faults:

1. Open or short transistor.
2. An open input to a gate causing the input to drift to a s-a-1 or s-a-0 condition (undefined).
3. An open gate transistor causing that device to drift to a permanent open or short condition. Electrically this is equivalent to mode 1.
4. Shorts between gate inputs or shorts from input to output. [23-24]

*Supported by Rome Air Development Center under Contract No. N-1-5520 for the project "Testability for VLSI".

In this paper, a new fault-model called conductance fault model is introduced which can represent modes 1, 2, and 3 mentioned above as well as leakage faults. It should be mentioned that mode 4 can be tested by a leakage-current testing setup. This principle has been used by Blore [12] to devise an efficient parallel testing procedure for CMOS.

There are several motivations for investigating a leakage-current based testing technique:

1. Extra testability generally requires extra pins which is a significant overhead. Leakage testing provides additional access by using already existing V_{DD} and V_{SS} pins [6].

2. In conventional testing, the site of fault has to be excited, and the effect of fault has to be propagated to the output pins. In leakage testing, propagation of the effect of the fault is automatic [13].

3. Leakage testing can provide transistor-level resolution as opposed to gate-level resolution in conventional testing.

4. Several important types of faults can be modelled as leakage faults. Some faults, like those caused by threshold drift, can be detected by leakage testing even before they start affecting the logical operation.

5. In CMOS devices, a short between two lines with opposite logic vaules will virtually present a short between V_{DD} and V_{SS}. This is because any logic 1(0) is connected through a low resistance path to V_{DD} (V_{SS}).

6. As explained below, shorting of certain transistors may not be detectable by conventional testing. They can be tested only by leakage testing.

7. The excessive leakage current is generally a few orders of magnitude greater than the normal leakage current. Excessive leakage is therefore easily identifiable.

8. Leakage testing can ensure that opens are not masked during opens test [6].

9. Since the excessive leakage currents are a few orders of magnitude greater than normal leakage currents, they can cause accelerated aging of affected areas within the chips.

The Conductance Model

The conductance fault model introduced below models switching and resistivity of the transistors. Since the model represents static behaviour, capacitances are not needed. As will be clear from the following discussion, it is more convenient to use conductance rather than resistance to characterize transistors. The model is based on these facts:

- An ON transistor has very high conductance (very low resistance) of about 10^{-1} ohm^{-1}.

- An OFF transistor can be represented by a leakage conductance. Ideally its value is 0, (infinite resistance), practically a normal transistor has a leakage conductance of the order of 10^{-12} ohm^{-1}. For an abnormal (leaky) transistor it can assume a value of 10^{-9} or higher.

- The gate is well isolated from the channel. Therefore, a transistor presents only a single path, from drain to source, for the leakage current.

The model is represented in Figure 1. It has an ideal switch which inserts either the ON conductance or the OFF conductance in the supply current path between V_{DD} and V_{SS}.

In the normal case, the ON conductance is very high and the OFF conductance is very low. We can now consider two possible situations for faulty behavior.

1. The ON conductance can be too low.. This corresponds to the situation when the path between V_{DD} and V_{SS} is open. This corresponds to stuck-open faults.

2. The OFF conductance can be too high. This will cause an excessive leakage current whenever appropriate V_{DS} ($V_{DS}=V_{DD}-V_{SS}$) is present. We term this a leakage fault. In the extreme case, when the abnormal OFF conductance approaches normal ON conductance, it corresponds to the stuck-on faults.

The stuck-open and stuck-on faults can occur in both MOS and CMOS devices. They were first identified by Wadsack [9]. Test generation for them has been considered in [2,10,19], simulation in [9,20] and testable design in [7].

Only leakage faults are considered here. They may not affect the logical operation of the circuit for some time, but eventually they are likely to turn into logical faults. Consider, for example, threshold drift due to migration of alkali ions [2]. Threshold drift causes the threshold voltages of P-type transistors to increase and N-type transistors to decrease. This will initially cause increased leakage, as the OFF conductance of N-type transistors increases. When the drift has advanced sufficiently, the OFF conductance of N-type transistors becomes very high (stuck-on) and the output to a gate essentially gets stuck at 0.

Because of its simplicity, the conductance model is suitable for simulation. If dynamic behaviour is also desired (for example, for handling the sequential behaviour of stuck-open faults), appropriate capacitances have to be added.

Testing by Measuring Leakage Current

The leakage current in CMOS is controlled by the OFF transitors with appropriate voltage across

them. By applying different input vectors to combinational circuits (input and state vectors for sequential circuits) different sets of transistors can be made to control the overall supply current. One can, therefore, measure the supply current under different vectors and then extract some information about the transistors from the data.

Example 1: Consider the NAND gate shown in Fig. 2. To keep the explanation simple, let us assume that the integrated circuit chip does not contain anything else. The overall conductance of the chip under each vector can be measured by measuring the supply current and dividing it by the supply voltage. If the OFF conductances of transistors NA, NB, PA, PB are represented by C(NA), C(NB), C(PA), C(PB), and if the measured conductances under input vectors 00, 01, 10, 11 are indicated by C_0, C_1, C_2, C_3, respectively, then the following conductance equations are obtained.

Vector		Unknowns		Measured Values
A	B			
0	0	$[C(NA)^{-1} + C(NB)^{-1}]^{-1}$	=	C_0
0	1	$C(NA)$	=	C_1
1	0	$C(NB)$	=	C_2
1	1	$C(PA) + C(PB)$	=	C_3

We thus obtain a set of equations where conductances of different transistors are unknowns. In the above set, values of C(NA) and C(NB) is given immediately. Since transistors PA and PB are in parallel, there is no way to distinguish between C(PA) and C(PB), and thus C(PA) + C(PB) should be treated as a single variable. The first equation is dependent on the rest and hence provides only redundant information.

After the conductances of different transistors or groups of transistors in parallel are obtained, it can be checked if they are less than a specified value. If the conductance of a transistor is greater than the maximum allowed, it can be regarded as faulty. Because of restricted experimental accuracy, the lower bound of acceptable range can neither be defined nor used.

The above procedure, which can be called equation-solving method, can easily be applied to individual NAND, NOR and inverter gates, as well as their fanout-free networks [14]. In general, however, several problems are encountered.

- Nonlinear terms may be involved, these will make solving the set of equations difficult to automate.
- If all possible vectors are used, a large number of equations are obtained. The equations are not, in general, linearly independent. After the redundant equations are removed, there might be fewer equations than variables. It is still possible to extract information from these equations. The equations can be considered as constraints and maximum and minimum values of variables can be obtained.

Transistors with minimum conductance values more than allowable maximum, are definitely leaky. Those with maximum conductance values, less than allowable maximum, are definitely normal. However, all this would require large computation time. An alternative way is to use set-theoretic methods based on probabilistic aspects of the problem [22].

Test Generation For Some Basic Structures

Like in conventional testing, test generation for leakage testing require two considerations. First is to sensitize the fault so that its affect can be examined. In leakage testing, a transistor is sensitized if it is OFF, and its terminals are connected to V_{DD} and V_{SS} through low resistance paths. If the transistor is leaky, it will present a low resistance path between V_{DD} and V_{SS} and high leakage current will flow. The second consideration is to minimize the test set. We define a minimal complete leakage test set (MCLTS) for a CMOS circuit as a minimal set of tests capable of generating the maximum possible information about transistor leakage conductances, i.e., capable of generating the largest set of independent equations containing conductances.

For very simple structures MCLTS can be generated in a simple way. Consider, for example, individual inverter, NAND and NOR gates. The transistor level diagram of these gates and their corresponding MCLTS's are given in Fig. 2. The stuck-at faults tested by the same tests are also included for comparison.

For individual complex cells, an algorithmic way to generate MCLTS's is possible. A graph-theoretic method is presented here [18]. Let us consider the electrical lines, the nodes in a graph, and let the transistors be the edges. A cut-set is a set of transistors, removal of which will divide the graph into two separate parts. For example, in Fig. 3, {AP,CP} and {CN,DN,EN} are two of the cut-sets. A set of independent cut-set generates independent equations. We will view the graphs as consisting of several subgraphs, called serial groups, all connected in series. In Fig. 3, there are four serial groups, consisting of the {AP,BP,CP}, {GP,DP}, {EP} and {AN,BN,CN,GN,DN,EN}. The test generation method consists of the following steps:

1. Identify all serial groups.
2. For each serial group, find the largest set of linearly-independent cut-set.
3. Generate a test vector for each cut-set such that the transistors in the cut-set are OFF and are connected to both V_{DD} and V_{SS} through a low-resistance path.

Example 2: For Fig. 3, the independent cut-sets are given below:

{AP,CP}, {BP,CP}

{GP,DP}

{EP}

{AN,BN,GN,EN}, {CN,GN,EN}, {CN,DN,EN}.

Consequently, a minimal CLTS is (in terms of A,B, C,D,E,G): 101000, 011000, 000101, 000010, 001100, 110100, 110001.

An important result for complex cells (NAND and NOR gates are special cases of it) is given below:

Theorem 1: For any individual complex cell, a MCLTS consists of n/2+1 tests, where n is the number of transistors.

Proof: Consider first the structure of complex cells. Starting from an inverter, any complex cell can be formed by a number of modification steps. In each step, two transistors (one P-type, other N-type), are added, one in parallel with a set of transistors (or a single transistor), and the other in series with the complimentary set of transistors in the complementary part. For a complex cell with n transistors (n-2)/2 such steps are needed. Q.E.D.

Each modification step adds only one additional independent cut-set. The transistor which is added in parallel to a set S of transistors, simply has to be added to all independent cut-sets of S. The transistor which is added in series to the complementary set of transistors S', will require an additional cut-set.

An inverter requires two cut-sets. The rest of n-2 transistors will add (n-2)/2 cut-sets. Thus the maximal number of independent cut-sets as well as the number of tests required, is 2+(n-2)/2 = n/2+1.

A MCLTS for a circuit consisting of a number of gates, complex cells, etc., will contain a MCLTS for each element. For such circuits, MCLTS can be obtained by considering all available test patterns, and then removing those which provide only redundant information. If an incomplete set of tests is available (for example, those generated for stuck-at testing), the set of undetected faults can be obtained by simulation. Additional tests for these undetected faults can be generated and added.

NAND, NOR and inverter-gates and complex cells provide a circuit that connects V_{DD} and V_{SS}. Conductances of these elements appear in parallel across V_{DD}-V_{SS} lines. The overall conductance is then simply the sum of conductances of all elements.

The transmission-gates can complicate the situation by creating cross-paths. A common transmission gate configuration is shown in Fig. 4. The transmission gate T($\overline{T}$) presents a low resistance path when CL=0(1) for either direction, otherwise, both transistors are OFF, and it presents a high resistance path. The voltage across $\overline{T}$ in Fig. 4(a) is always zero in a static situation, hence it will never contribute to overall conductance. The transistors in $\overline{T}$ cannot be tested for leakage faults. The leakage in the transistors in T can be tested if it is OFF, and outputs of I_1 and I_3 (since $\overline{T}$ is ON) are of opposite logical values. The conductance of transistors in T will appear across V_{DD} and V_{SS}, in parallel with other elements.

Relationship Between Logical Testing and Leakage Testing

It is important to consider the relationship between logical and leakage testing. Let us first consider only networks consisting of inverter, NAND and NOR gates.

Each gate consists of a set of several elements (s.e.) which are transistors or a parallel combination of transistors. As no distinction can be made among a set of parallel transistors, they are regarded as a single s.e. Each s.e. allows a small leakage current when it is OFF.

Theorem 2: For an independent NOT, NOR or NAND gate, the minimum stuck-at fault test-set is the complete leakage test-set (test-set which enables the leakage current of each s.e. to be determined). From this set each test pattern tests one s.e. for leakage current as well as one stuck-at fault set containing at least one unique fault not tested by other vectors.

Proof: The proof is apparent when one considers the tables in Fig. 2. For example, A stuck-at-1 is only testable by AB=01 for the NAND gate.

Corollary 1: For a NOT, NOR or NAND gate, whenever the leakage current is determined by a single serial element, the corresponding stuck-at fault-set is tested and vice-versa.

Now let us consider a leakage test experiment. Each gate constitutes a parallel path for the total leakage current. For any jth vector the total measured leakage conductance includes the contribution from each gate:

$$\sum_i \text{(contribution from gate i under vector j)} = C_j$$

Contribution from each gate would either be controlled by a single s.e. or by a series combination of s.e. For a gate, let the leakage conductance due to the kth s.e. or unique series combination of serial elements be denoted by C_k. Then a v by s matrix M, consisting of 1's and 0's can be written such that

$$M \cdot C_k = C_j \qquad (1)$$

where v is the number of input vectors and s is the total number of serial elements and unique series combinations of all gates. An element of M, m_{kj}=1 whenever k^{th} element contributes conductance when j^{th} vector is applied, 0 otherwise,

$k = 1,2,\ldots,s$ and $j = 1,2,\ldots,v$.

Example 1 shows the set of equations for $v = 4$, $s = 4$. The first equation contains a series combination of serial elements. The last equation deals with the contribution from a serial element consisting of PA and PB in parallel.

Eq (1) is a system of linear equations in C_k's. Now we will show that for a minimal stuck-at fault test-set, the resulting system of equations is linearly independent. We will do so by considering only those columns of M which correspond to a single s.e. If the rows of M are linearly independent when some of the columns are not considered, then they are also linearly independent with all the columns. Let us form a matrix M* which has only those columns of M which correspond to the s.e.'s of all gates. For instance, in Example 1, the M* contains columns corresponding to elements NA, NB, and the parallel combination of PA and PB.

Theorem 3: If M* is obtained for a minimal stuck-at fault-test set, then all its rows are linearly independent.

Proof: Consider a vector p (corresponding to a row), it must test at least one stuck-at fault f_1 which is not tested by any other. The fault f_1 corresponds to the leakage conductance controlled by a specific s.e., and hence the corresponding row of M* has a 1 in the corresponding place. No other row can have a 1 in this column, because it would mean that another test-vector, say q, would cause contribution of this s.e. to its total leakage conductance, which in turn would mean that q also tests f_1.

Since each row of M* has a 1 in a column, where no other row has a 1, all the rows are linearly independent. Q.E.D.

If a stuck-at test set is available which is minimal and complete, then by Theorem 3, all equations generated will be linearly independent, and by Corollary 1, all s.e. will be tested (i.e., their conductance will appear in the total conductance measured). This leads us to the following important result:

Theorem 4: For a network consisting of only inverter, NAND and NOR gates, a minimal complete stuck-at test-set will generate a set of equations in which (i) all equations are linearly independent and (ii) each variable will appear at least once.

This suggests that for such networks, a minimal stuck-at test-set can be used as a starting point for generating a MCLTS. This also indicates that leakage testing and logical testing based on stuck-at fault-model can be done at the same time since a large fraction of vectors are good for both.

Correspondence between logical and leakage testing is even better if stuck-open and stuck-on fault model is used (which is perhaps more appropriate for MOS and CMOS because:

- A logical test, which tests for a stuck-open transistor, will turn its complimentary transistor OFF, with about V_{DD}-V_{SS} potential across it. It is, therefore, a leakage test for the complimentary transistor.

- The stuck-on faults are not always testable by logical testing. In order to excite a stuck-ON transistor, a vector is necessary to turn the transistor-under-test OFF, and tc connect its terminals to V_{DD} and V_{SS} through low resistance paths. If the transistor is indeed stuck-ON, the output of the gate or complex cell containing this transistor, will be connected to both V_{DD} and V_{SS} thrcugh low resistance paths. The logical output can then be either the same as or different from the normal output depending on the resistances involved. Generally, stuck-ON faults in the load part cannot be detected by logical testing [20]. Leakage testing is very effective in this case. Any stuck-ON fault will be automatically tested when the complimentary transistor is tested for stuck-open faults.

Therefore, leakage testing can be effectively and naturally combined with logical testing for stuck-open faults.

Analysis of Experimental Data

In order to evaluate the effectiveness of leakage testing, a probabilistic analysis of the problem is required. This requires analysis of experimental data. Some data is available from "Digital Microcircuit Characterization and Specification" [17]. It includes device description and supply current data for five CMOS devices. Several samples of each device were examined for logical integrity and leakage current under different vectors. All had logically correct performance but the leakage current was excessive in some cases. We analyzed the data to seek the following information.

1. Identify possible leaky transistors.

2. Calculate the average normal leakage conductance and its variance.

3. Find the distribution of abnormal leakage conductance.

The average normal conductance per-transistor for a chip can be determined by using either Procedure A or Procedure B given below. It is assumed that all normal transistors within a chip have about equal conductance, as is suggested by the experimental data. Some transistors may have dimensions different from the rest, their conductance will be different from others. This fact can be taken into account if desired, but can be ignored without significantly affecting the accuracy. For simplicity, the effect of protection diodes is also ignored here.

Procedure A:

1. Assume each transistor has a unit conductance of G ohm^{-1}.

2. For any specific input vector V_i, the transistor level diagram can be used to compute the total conductance. Let it be equal to $N_i G$ where N_i is not necessarily an integer.

3. For this same vector V_i, let the measured conductance be C_i. Then for V_i the average conductance per transistor is given by

$$G = C_i/N_i$$

4. Steps 2 and 3 are repeated for all vectors, and the resulting values are averaged.

The disadvantage of Procedure A is that a lot of work is required because the entire circuit has to be analyzed for each input vector. An approximate procedure can be found which requires significantly less work because only one element of each kind has to be analyzed for all input vectors of that element. This, called Procedure B here, is based on the following observations:

1. Experimental data shows that the total normal conductance is about equal for all vectors [17].

2. The transistor level diagrams for several circuits such as BCD-to-Decimal decoder, a section of ALU, were analyzed for all input vectors. For each circuit, assuming all transistors have equal conductance, the total conductance was found to be about equal for all vectors.

We can, therefore, reasonably assume that in general , for devices with more than just a few gates, all N_i are about equal. The assumption should be even better for larger devices, since the sample size is greater, and the average should be closer to the expected value. Exceptions to this may be possible for devices with very regular structure and regular signal values. Such cases can be handled by Procedure A.

Procedure B:

1. Identify basic elements such as gates, complex cells, etc. The total conductance of the device is equal to the sum of the conductances of the individual elements.

2. For each element, find conductances for all V_i and average them to find average conductance. This, of course, assumes that the occurence of all vectors are equally likely.

3. The approximate average conductance for a chip is given by the sum of average conductance of all its elements. Let this be equal to MG, where M is a positive number, not necessarily an integer.

4. The average conductance per transistor is then given by

$$G = \frac{\text{average of measured conductances}}{M}$$

Steps 1 and 2 have been carried out for a number of commonly used elements. Analysis for inverter, NAND and NOR gates is presented here. For the elements shown in Fig. 5 [18], only the results are presented here.

Inverter: For an inverter only two input vectors, 0, and 1, are possible. The conductance in both cases is G, hence the average conductance is G.

NAND and NOR gates with n inputs: One input vector will turn all parallel transistors OFF giving conductance equal to nG. There will be $_nC_k$ input vectors which will turn k series transistors off, providing conductance of G/k, where k=1,2,...,n. The average conductance is then

$$\frac{1}{2^n}\left\{n+\sum_{k=1}^{n}\frac{n!}{k!(n-k)!}\frac{1}{k}\right\}G.$$

For example, for 2,3, and 4-input NAND or NOR gates, the average conductance is 1.125G, 0.979G and 0.786G respectively.

Transmission-gate groups: Four common configurations involving complimentary pairs, shown in Fig. 5 a,b,c,d have average conductance of G, 2G, 0.66G and 0.8G respectively. Fig. 5e shows a group in which only one is ON at a time. The average conductance is (N-1)G, where N is the number of transmission gates. If it is allowed for all N transmission gates to be OFF, then the average conductance is NG.

Complex cells: In general, each complex cell has to be analyzed separately. For the complex cell of Fig. 5f, the average conductance is 1.75G.

Connected-AND and connected-OR: These structures, shown in Fig. 5g and h have average conductance of 0.5G.

Example 3: We will use the data for 4028 BCD-to-Decimal decoder as an example. Fig. 6 shows the circuit diagram and the experimental data. The table shows the leakage current (in nanoamperes) for the five 4028 chips used for a supply voltage of 15 volts.

Average conductance (Procedure B)

26 inverters	26 x 1
4 2-input gates	4 x 1.125
6 3-input gates	6 x 0.979
12 4-input gates	2 x 0.786
	M = 37.94

It can be seen by inspection that the chips #1, #2 and #3 show only normal leakage currents. Chip #3 shows normal leakage of 1.13 nA and abnormal leakage of about 1.73×10^5 nA. Since the

abnormal leakage values are about the same (allowing for limited measuring accuracy), it is likely that they are caused by a single transistor. Chip #4 shows normal leakage of about 0.462 nA (average) and abnormal leakage of 2.9×10^{5}.

The normal conductance per-transistor can be obtained by dividing the average normal leakage current by 15 volts x 37.94. The values are obtained as (in ohm^{-1}): 3.19×10^{-13}, 8.78×10^{-12}, 1.98×10^{-12}, 8.12×10^{-13}, 3.58×10^{-13}.

As the abnormal leakage current is assumedly caused by a single transistor in both cases, the abnormal transistor conductances for Chips #3 and #4 are obtained, respectively, by dividing the abnormal leakage current values (1.75×10^{5} nA and 2.9×10^{5}nA) by 15 volts: 1.15×10^{-5}, 1.93×10^{-5}.

For both Chips #3 and #4, it is possible to identify a small set of transistors which includes the leaky transistor. For Chip #3, it can be seen that excessive leakage of about 1.7×10^{5}nA occurs whenever Ouptut line 0 is logically 0. When output line 0 is logically 1, excessive leakage does not occur. Assuming that a few transistors are more likely to be faulty than a large number, we can suspect that there is leaky transistor in the three gates associated with the output 0. As the faulty transistor is sensitized, when the output 0 is logically 0, the leaky transistor is sensitized (i.e., normally OFF) when input vector 0000 is applied. The suspected transistor set (STS), then, can be narrowed down to {N-type in inverter G4, P-type in inverter G5}. The NOR gate in series with G4 and G5 would produce the effect only if all three series transistors are leaky. The faults in the STS are equivalent, no distinction can be made between them.

Similarly for Chip #4, the STS is {N-type transistors in NOR G1, P-type in inverter G2, N-type in inverter G3}.

By analyzing the data for the five devices, distributions for normal and abnormal transistors were obtained, which are shown in Fig. 7. The Y axis for normal conductances per transistor is the number of chips, for abnormal transistor conductances, it is the number of transistors. It should be noted that the distribution for normal transistors represent more than 4500 transistors whereas the distribution for the abnormal transistors represents only 16 transistors.

Some important features of the distributions in Fig. 7 should be noted. The distribution of normal transistors is very asymetrical (notice the logarithmic scale). A Gaussian distribution cannot be used here, perhaps a fit with Weibull or Gamma distribution can be obtained. The distribution for abnormal transistors is not smooth because of insufficient data. Still it can be noted that the distribution is very wide and it is also asymetric. Between the normal and abnormal distributions, there is a very significant gap, about three orders of magnitude wide. This distinction between normal and abnormal leakage values provides resolution for the leakage testing method. The parameter values would obviously depend on the manufacturing technology used.

Summary

A new fault model, called conductance-fault model for CMOS integrated circuit is introduced. The significance of testing by measuring leakage current is pointed out. Relationship between the fault model and stuck-open, stuck-on and leakage faults is given. Information extraction by solving a set of equations is introduced and associated problems are considered. Testing basic structures like NAND, NOR, inverter gates, complex cells and transmission gates is examined. Relationship between leakage and logical testing is considered. Results of analysis of some experimental data are reported.

Acknowledgment

The authors would like to thank Dr. Mark Levi, who initiated the investigations into testing by measuring leakage current, for his comments and suggestions.

References

1. S. Calebotta, "CMOS, The Ideal Logic Family", Application Note, CMOS Data Book, National Semiconductor, 1978, pp. 6.3-6.10.

2. Y.M. El-zig, "Automatic Test Generation for Stuck-Open Faults in CMOS VLSI", Proceedings of the 18th Design Automation Conference, 1981, pp. 347-354.

3. D. Fullagar, "CMOS Comes of Age", IEEE Spectrum, December 1980, pp.24-27.

4. D.L. Wallesen, "CMOS LSI - The Computer Component Process of the 80's", IEEE Computer, February 1980, pp. 50-67.

5. S.Z. Szirom, "Custom-Semicustom IC Business Report", VLSI January/February 1982, pp. 32-38.

6. M.W. Levi, "CMOS is Most Testable", Proceedings of the 1981 International Test Conference, 1981, pp. 217-220.

7. J. Galiay, et.al., "Physical versus Logical Fault Models MOS LSI: Impact on their Testability", IEEE Transactions on Computers, Vol. C29, No. 6, June 1980, pp. 527-531.

8. G.R. Case, "Analysis of Actual Fault Mechanisms in CMOS Logic Gates", Sandia Laboratories Report SAND 75-0621.

9. R.L. Wadsack, "Fault Modeling and Logic Simulation of CMOS and MOS Integrated Circuits", Bell System Technical Journal, May-June 1978, pp. 1449-1474.

10. Y.M. El-zig and R. Cloutier, "Functional-Level Test Generation for Stuck-Open Faults in CMOS

VLSI", Proceedings of 1981 International Test Conference, Philadelphia, October 1981, pp. 536-546.

11. R.S.C. Cobbold, Theory and Applications of Field-Effect Transistors, Wiley-Interscience, New York, 1970.

12. R.A. Blore, "Parallel Testing for CMOS Microelectronics", Proceedings of 1980 International Symposium for Testing and Failure Analysis, Los Angeles, October 1980, pp. 247-249.

13. C.C. Timoc, Personal Communication, October 1981.

14. The second status report for the project "Testability for VLSI", School of Advanced Technology, SUNY Binghamton, September, 1981.

15. The third status report for the project "Testability for VLSI", School of Advanced Technology, SUNY Binghamton, October, 1981.

16. The fourth status report for the project "Testability for VLSI", School of Advanced Technology, SUNY Binghamton, November, 1981.

17. M. Ostrowski, "Digital Microcircuit Characterization and Specification", General Electric Company report for Rome Air Development Center, August, 1975.

18. The seventh status report for the project "Testability for VLSI", School of Advanced Technology, SUNY Binghamton, February, 1982.

19. K.W. Chiang and Z.G. Vranesic, "Test Generation for MOS Complex Gate Networks", Proc. 12th International Symposium Fault-Tolerant Computing, June 1982, pp. 149-157.

20. A.K. Bose et.al., "A Fault Simulator for MOS LSI circuits", Proc. 19th Design Automation Conference, June 1982, pp. 400-409.

21. D.G. Edwards, "Testing for MOS Integrated Circuit Failure Modes", Digest 1980 International Test Conference, Nov. 1980, pp. 407-416.

22. The tenth status report for the project "Testability for VLSI", School of Advanced Technology, SUNY Binghamton, May, 1982.

23. S. Xu and S.Y.H. Su, "Testing Feedback Bridging Faults Among Internal, Input and Output Lines by Two Patterns", Proceedings of the 1982 International Conference on Circuits and Computers.

24. M. Karpovsky and S.Y.H. Su, "Detecting Bridging and Stuck-at Faults at Input and Output pins of Standard Digital Components," Proc. of 17th Design Automation Conference, October, 1980, pp. 484-505.

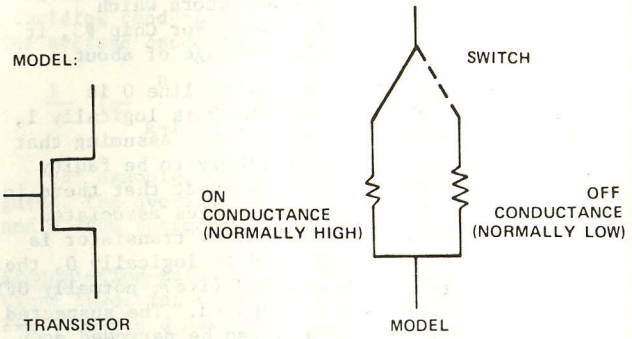
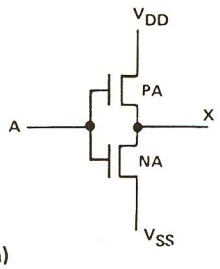
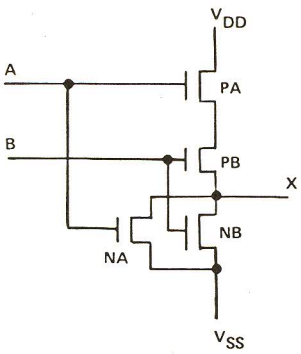


Figure 1: The conductance fault model



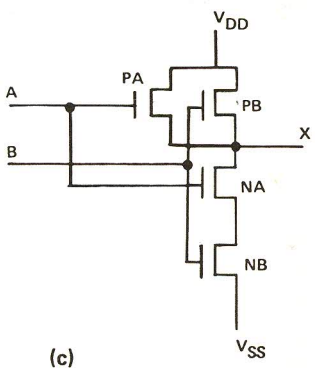
(a)

Input A	Stuck-at Fault Set	Leakage Determined By
0	A-1,X-0	NA
1	A-0,X-1	PA



(b)

Inputs A	Inputs B	Stuck-at Fault Set	Leakage Determined By
0	0	A-1,B-1,X-0	P(NA,NB)
0	1	B-0,X-1	PB
1	0	A-0,X-1	PA
1	1	X-1	S(PA,PE)



(c)

Inputs A	Inputs B	Stuck-at Fault Set	Leakage Determined By
0	0	X-0	S(NA,NB)
0	1	A-1,X-0	NA
1	0	B-1,Y-0	NB
1	1	A-0,B-0,X-1	P(PA,PB)

Figure 2: Examination of (a) inverter (b) NOR (c) NAND gates.

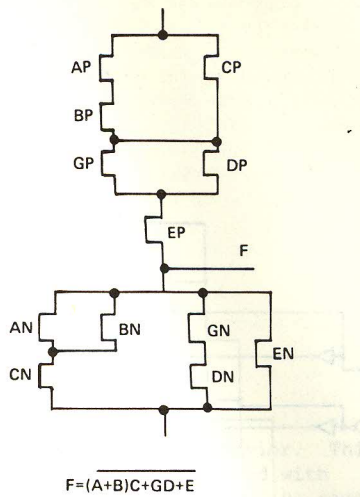


Figure 3: A Complex cell

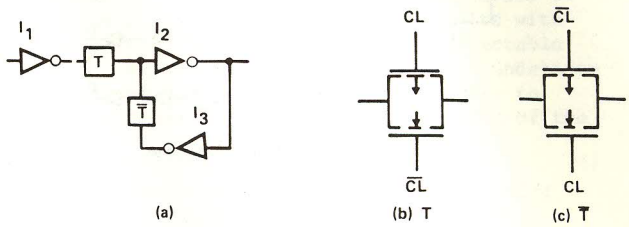


Figure 4: A common transmission-gate structure

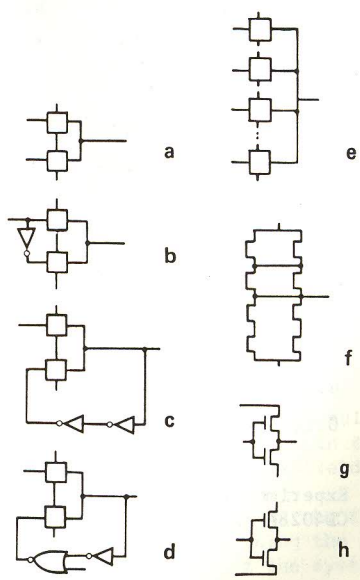
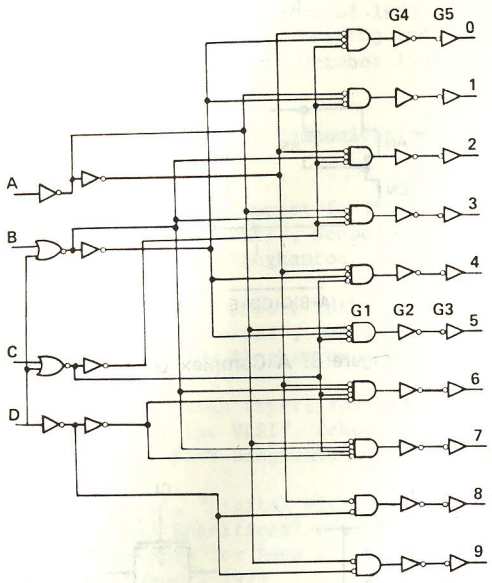


Figure 5: Common CMOS elements



BCD to Decimal Decoder

Leakage Current for Different Chips

Vector D C B A	Chip #1	Chip #2	Chip #3	Chip #4	Chip #5
0 0 0 0	0.18	4.7	1.13	0.44	0.20
0 0 0 1	0.18	5.1	1.75×10^5	0.46	0.20
0 0 1 0	0.18	4.5	1.75×10^5	0.42	0.19
0 0 1 1	0.18	4.8	1.75×10^5	0.45	0.21
0 1 0 0	0.18	4.9	1.75×10^5	0.45	0.21
0 1 0 1	0.19	5.8	1.75×10^5	2.9×10^5	0.22
0 1 1 0	0.18	5.0	1.7×10^5	0.46	0.20
0 1 1 1	0.195	6.0	1.7×10^5	0.55	0.21
1 0 0 0	0.17	4.4	1.7×10^5	0.45	0.20
1 0 0 1	0.18	4.8	1.7×10^5	0.48	0.20

Fig. 6: Experimental data (in nanoamperes) for CD4028A chips.

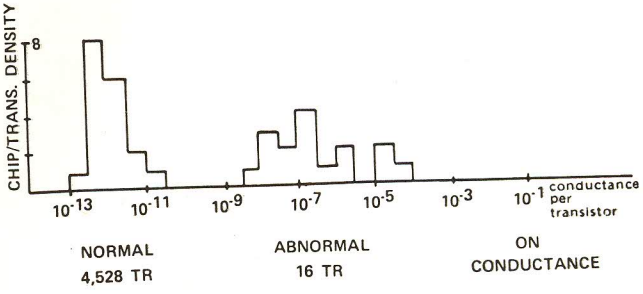


Figure 7 : Distributions of Normal and Abnormal conductances