X-IDDQ: A Novel Defect Detection Technique Using IDDQ Data

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Abstract

A statistical technique X-IDDQ for extracting defect information from IDDQ data is presented that is effective for detection of defects in ICs. The technique treats the IDDQ measurements in a holistic manner to come up with a statistic X that is highly correlated to the presence of defects. X-IDDQ facilitates binning of ICs and enhances the test process by early identification of faults. The transformation metrics, for evaluating X statistic from IDDQ measurements, obtained using one batch works extremely well for different batches, facilitating its use with manufacturing-line testing.

Keywords: Binning, IDDQ, Defect Correlation, Test Optimization, Principal Component Analysis.

1. Introduction

Operational tests such as functional test verify the functionality of a chip while structural tests like stuck-at, delay, and IDDQ rely on the circuit structure for defect detection. A SEMATECH study [14] was undertaken to determine the relative effectiveness of different testing methodologies. Although some defective ICs were detected by more than one test methods, the study concluded that all test techniques uniquely detected some class of defects and none of them might be dropped in favor of some other technique [15]. Manufacturers, therefore, need a variety of tests in their test suite to screen defective ICs. Some strategies aiming to improve the efficiency [4] and optimization of test [19] have been proposed.

Although a significant fraction of devices that fail stuck-at, functional and delay tests are also identified as faulty by IDDQ testing [13], IDDQ testing is performed primarily to detect those faults (such as reliability faults) that are not detected by other methods of testing. Furthermore, IDDQ based test approaches in general have relied on elevated IDDQ or Delta-IDDQ values to identify the potentially faulty devices. However, it has been argued that IDDQ-fail only devices may not be really faulty devices if they do not violate any functional or structural specifications**.**

In this paper, we provide results indicating an extremely strong correlation, far beyond what has been known, between the set of IDDQ measurements of a device and the presence of stuck-at, functional and delay faults in a device. The correlation becomes evident with a test statistic, X (a discriminant factor used for information extraction), obtained by using a Principal Component Analysis (PCA) based transformation of the IDDQ measurements. The proposed approach uses the distribution of X values in a batch of devices to group the devices into three bins: High Defect (HD), Intermediate Defect (ID) and Low Defect (LD). Using this binning technique, the tester can select potential devices for more extensive testing while rejecting some as faulty devices thus reducing test effort, time and resources. The correlation observed between X statistic and the non-IDDQ faults leads us to a novel technique, X-IDDQ, that helps in defect detection by screening out early failures using IDDQ data. In doing so, we reduce the test resources that would otherwise be required to test these devices.

We also show that the transformation metrics, for evaluating X statistic from IDDQ measurements, obtained using one batch works extremely well for different batches of same component. Thus the transformation can be pre-computed based on an initial set of devices facilitating on-line binning. Results from SEMATECH data also indicate that the IDDQ-only fail devices in High Defect bin have extremely low probability of passing burn-in tests.

With the increasing quiescent current levels, IDDQ based tests lose their defect screening resolution if a fixed threshold is used. Because of its unique capability of detecting defects such as resistive shorts that have become more likely for advance technologies [12], manufacturers consider IDDQ an integral part of

their test suites for screening reliability-risk devices. To retain the effectiveness of IDDQ testing in deep submicron technologies, many solutions have been proposed [10,17]. To achieve quality levels of 100 DPM (Defects per Million units) in nanometer ASICs, it has been suggested that defect based test methods which focus on outlier identification from test data such as IDDQ are a critical component [2]. Our technique extends the concept of identifying outliers by binning faulty devices separately thereby optimizing testing strategy.

The paper is organized as follows. The X statistic based on Principal Component Analysis is introduced in Section 2. Section 3 discusses the SEMATECH data set used and its attributes. The results presented in the next section demonstrate the strong correlation between the X statistic, and the non-IDDQ faults. We next evaluate the devices that failed only the IDDQ test based on their membership in different bins, and the impact of burn-in on them. Section 6 explores the choices in implementation of the proposed binning scheme, and the use of transformation metric from one batch for binning a different batch. Section 7 concludes the paper and highlights future work.

2. X statistic

Achieving higher resolution in the presence of a large background current requires using multiple measurements and careful extraction of abnormal IDDQ patterns that may signal the presence of a defect. The measured IDDQ values under different test vectors are known to be correlated [3] for a single device. Because of this correlation, Principal Component Analysis (PCA) can be used to extract information components from such data and represent them using fewer new variables. PCA is a mathematical technique that transforms a number of correlated variables into a set of less correlated variables called principal components (PCs) [1,3,11].

If the number of principle components is p = 15, then each device is now characterized by fifteen z-score values instead of fifteen IDDQ values and so z-scores are the new coordinates of the IDDQ values of a device in the space of principal components. The transformed variables are principal components and the individual transformed observations are termed as the z-scores. However, each of the fifteen z-score values for a device is a linear combination of all the corresponding IDDQ values for that device.

For any given data set, outliers are viewed as observations, devices in our case, that are inconsistent with the remainder of the data/devices. Hence, in the case of a p-variate data, such as IDDQ data, this definition implies that outliers are a long way from the rest of the observations in the p-dimensional space defined by the variables. Several methods have been suggested for detecting outliers and some of these methods use PCs [11]. Detection of outliers can be complicated since they can be of various types, the first few and the last few PCs are known to detect different types of outliers.

We have derived a test statistic X_i, suitable for IDDQ based testing, by modifying a test statistic suggested in [9]. X_i is computed as shown in equation (1). PCs are known to have decreasing variance with increasing index. Hence to give the components equal weight, the variance of the k^{th} sample PC, l_k is used for normalization. The sample variances of $z_{ik}/l_k^{1/2}$ will all be equal to unity. Due to the extreme range of X_i values, we have modified the statistic by using a logarithmic transformation.

$$X_i = \log_{10}\left(\underset{p-q+1 \le k \le p}{Max} \left| \frac{z_{ik}}{\sqrt{l_k}} \right| \right) \quad \text{..... (1)}$$

where z_{ik} is the value of the k^{th} PC for the i^{th} observation, p is the total number of PCs (the number of IDDQ vectors used) and q is the selected number of least significant PCs.

X_i identifies the values that are 'outliers' with respect to correlation structure of the data. Higher the value of this test statistic, more the extremity of this observation from the data set. This X statistic could be applied to any IDDQ dataset for defect detection in ICs and therefore this technique is called X-IDDQ. This paper demonstrates the effectiveness of this technique by applying it to the SEMATECH dataset.

3. Application to SEMATECH data

Table 1. Classification of devices

Category	SEMATECH Sort-Code Key
All Pass (AP)	$$
All Fail (AF)	AF, IO, RR, SR
Delay Fail (DF)	1P,2F, 3F
Functional Fail (FF)	1F, 2A, 2D, 3I, 3T
Stuck-at Fail (SF)	1T, 2B, 2C, 2E, 3P
IDDQ-only Fail (IF)	1I

The SEMATECH study [14] involved a 116K-gate standard graphics controller chip designed in IBM Phoenix CMOS4LP technology. 18,466 devices in the study underwent four tests: stuck-at fault, functional, delay and I_{DDQ}. 195 vectors were used for IDDQ measurements on five lots containing 5814, 1003, 2638, 2561 and 6450 devices. Our analysis includes only the observations on devices at wafer-level. Furthermore, each device was assigned a sort-code key based on the test results. For simplicity in analysis, we

classified the devices into 6 mutually exclusive categories as shown in Table 1. Each category includes devices with the designated sort-code key assigned. As each device was assigned only one sort key, they are mutually exclusive. A small percentage of devices with sort key IO, RR, SR were included in AF category.

In the X-IDDQ technique, the steps taken to find X values for devices are as follows.

1. Determine transformation matrix which gives us the principal components, using the IDDQ data.
2. Find the z-score values of all devices in the lot.
3. Obtain the X value of all devices by choosing q.
4. Arrange the devices in a lot in decreasing order of X values.

The X values are then used for binning devices into the three bins: HD, ID and LD. The next section, examines the devices separated into three bins.

4. Detection of non-IDDQ faults

Lot 1, with 5814 devices, was used to form a good sample for the initial investigation of the proposed technique. Due to the common industrial practice of taking only 20-30 IDDQ observations for each device, all the 195 IDDQ observations in the SEMATECH study are not considered. Only the first 15 IDDQ observations of each device are considered. They constitute the IDDQ data matrix (M). To estimate PCs ($M=USV^T$ using Singular Value Decomposition theory [11]), the data matrix M includes only 15 IDDQ observations of 3507 AP devices in Lot 1. This is done to limit the outliers in the training set that can bias the estimation of PCs. In step 2, the data matrix M includes 15 IDDQ observations of all 5814 devices. The z-score values of all devices in the lot are then obtained ($Z=MV$ [11]). With $p = 15$ in equation (1), we use all the PCs ($q=p$) to estimate X for each device. The devices are then arranged in decreasing order of X values.

Figure 1 shows the plot of cumulative distribution function of X values. The value on the x-axis is the X value of the devices. On y-axis, F(X), is the proportion of devices in the lot with X values less than or equal to a specific value of X. Evidently, only 30% of devices have X values greater than 0 and 60% of devices have X values less than -3. Observing the plot, it is apparent that the devices fall into 3 different regions.

Devices with higher value of X are outliers compared to the remaining devices. This indicates the presence of defect(s) in the device that could cause it to have an IDDQ profile significantly different from the others. The probability that a device is defective will increase with the value X. Based on the curve, the devices can be grouped in 3 different bins based on their X values. In this investigation, a simple binning technique is employed where in the bin size is obtained by dividing the range of X values into three bins. The bins are called High Defect (HD), Intermediate Defect (ID) and Low Defect (LD) bins. Even though an extremely simple scheme is used here to identify the different bins, it is sufficient to demonstrate the effectiveness of the proposed approach. Bin HD includes devices with X values in the range of [X_{max}-*Bin_size*, X_{max}]. Bin ID includes devices with X values within the range [X_{min}+*Bin_size*, X_{max}-*Bin_size*] and the remaining devices fall in Bin LD.

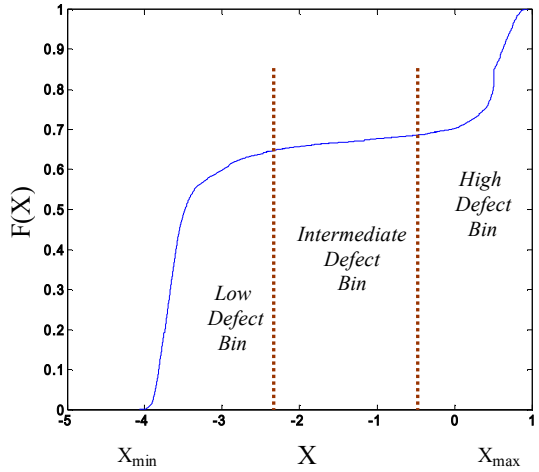

Figure 1. Cumulative distribution of X (lot 1)

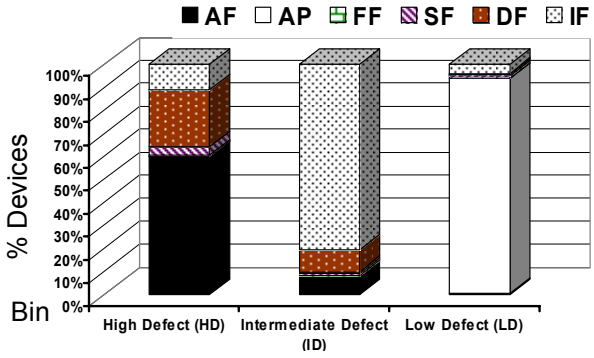

Figure 2. Binning results in lot 1 with p=q=15

Figure 2 shows the results of the binning with 1853, 214, and 3747 devices are in Bin HD, ID and LD respectively. The y-axis gives us the percentage of devices from the 6 categories in each bin. For instance, out of 1853 devices in Bin HD, 55% fail all tests (AF), 10% of fail only IDDQ tests (IF), 20% fail delay test, 5% fail Stuck-at tests. 80% of devices in Bin ID are IDDQ-only fails (IF). And almost 95% of devices in Bin LD pass all tests (AP). This demonstrates significant correlation between the faulty devices and

high X values. Bin HD with the highest X values contains only devices that fail voltage, delay and IDDQ tests. Thus X becomes a measure of the defect level in a device.

Similar steps were taken to bin devices in the remaining four lots, with one difference. To compute the z-score of all devices, the PC weights (transformation matrix V) from Lot 1 were used. The cumulative distribution function plot of X values of devices in these lots was similar to Figure 1. The results are displayed in Table 2. Note that the results in the table corresponding lot 1 correspond to those in Figure 2.

For each lot, the number of devices from each category that fall in the respective bins is reported. Sum of all devices in these bins equals the total number of devices in the lot. All the lots show a similar pattern in the results. Bin HD contains only devices that fail all or a combination of tests. The defect level of devices in this bin is definitely high. Conversely, Bin LD records a lower defect level with a majority representation of devices that pass all tests. In between, a few devices that fail some tests fall in Bin ID.

These results clearly indicate that the statistic X, derived using only the IDDQ data, has the capability of screening devices with defects leading to non-IDDQ faults (delay, functional or stuck-at) , a fact that is demonstrated by results in Table 2.

Table 2. Results using V from lot 1

Lot 1 – 5814 devices						
Bin	**AF**	**AP**	**DF**	**FF**	**SF**	**IF**
HD	1116	0	454	6	67	210
ID	17	0	20	2	2	173
LD	18	3507	20	32	33	137
Lot 2 – 1003 devices						
HD	240	0	59	3	17	39
ID	7	0	9	1	3	52
LD	6	494	21	1	7	44
Lot 3 – 2368 devices						
HD	330	0	132	2	17	51
ID	12	0	9	2	4	114
LD	17	1779	45	46	20	58
Lot 4 – 2651 devices						
HD	373	0	136	23	28	59
ID	16	0	17	27	7	124
LD	30	1509	55	76	46	35
Lot 5 – 6450 devices						
HD	906	0	348	7	29	165
ID	44	4	60	10	7	341
LD	43	3970	274	83	72	87

To compare the non-IDDQ defect screening of the Delta-IDDQ [18] and X-IDDQ technique we revisit the results of Lot 5 in Table 2. To implement Delta-IDDQ, only the first 15 IDDQ observations of each device are considered, just like in the application of the proposed approach in the previous section. Table 3 gives us the number of Delta-IDDQ (highlighted in bold) failed in each bin. The result can be interpreted in the following manner. Only 534 out of 906 AF devices in Bin HD are rejected by Delta-IDDQ. This implies that Delta-IDDQ fails to reject the remaining 372 AF devices in this bin, even though they fail voltage and delay tests. X-IDDQ however assigns these devices higher X values. In other instance, all 4 AP devices in Bin ID are rejected by Delta-IDDQ. X-IDDQ assigns these 4 AP devices, with abnormal IDDQ pattern, higher X values than the other AP devices that lead the former in Intermediate Defect Bin (ID).

Delta-IDDQ assumes that there is at least one vector in the set that activates the defect and the defective IDDQ is therefore higher than the fault-free IDDQ. Thus it is unable to screen devices with passive defects in which the profile of IDDQ values change without introducing a large Delta-IDDQ. Our proposed technique, on the other hand, calculates X values that are extracted from the IDDQ measurements of the entire lot and not just multiple measurements on the same device. Moreover, for the same number of IDDQ measurements as taken in Delta-IDDQ, the proposed X-IDDQ technique provides better defect detection.

Table 3. Devices that fail Delta-IDDQ in lot 5

Lot 5					
Bin	**AF**	**AP**	**DF**	**FF**	**SF**
HD	**534**/906	0	**253**/348	**5**/7	**20**/29
ID	**26**/44	**4**/4	**33**/60	**7**/10	**4**/7
LD	**18**/43	**1777**/3970	**111**/274	**32**/83	**27**/72

5. Analysis of IDDQ-only fail (IF) devices

IDDQ-only fail (IF) devices are those devices that pass Stuck-at, Functional, Delay test but fail IDDQ test. The SEMATECH study chose 5uA as the threshold limit to decide IDDQ pass/fail. If any device had an IDDQ observation greater than this limit, the device was rejected. The threshold selection for IDDQ testing is somewhat arbitrary, and often is chosen to limit yield loss as opposed to based on physics of failures. A few studies have been done [5,16] to understand these IF devices and further investigate the question of whether or not reject these IF devices during testing. This issue is important to manufacturers as rejecting these devices would lead to unjustified yield loss and thereby revenue loss. IDDQ test is capable of detecting unique latent defects including electromigration-induced defects, metal slivers, hot carrier injection damage [7] that can pose a reliability risk. It has also been shown that defects may exist that

can cause IDDQ failures but not cause functional failures [8]. Therefore, if the IF devices are shipped, they may fail later in the system and resulting in customer returns that would lead to costs related to replacement of the defective device and manufacturer's reputation [6].

In Table 2, there is a presence of IF devices in all 3 bins. No precise trend in increase/decrease of the number of these devices from Bin HD to LD is observed. It is essential to investigate the differences in defect characteristics of IF devices in the 3 bins. A device is categorized as IF simply because it exceeded the 5uA current limit. Now we examine the hypothesis that IF devices in Bin HD are likely to be devices with faults or reliability faults, while IF devices in Bin LD are likely to be otherwise fault-free devices.

Let us now investigate the reliability of these IF devices by looking at the burn-in results. In the SEMATECH study, devices that failed at least one of the test, but not all tests at wafer level, were subjected to tests after packaging and again after they underwent 6 hours of burn-in at 140°C and 1.5 times nominal V_{DD}. The following analysis only includes IF devices that underwent 6 hours of Burn-in.

Figure 3 shows that only a small percentage of IF devices in Bin HD eventually pass all tests after burn-in. The increase in reliability of devices from Bin HD to Bin LD is seen in all lots. Thus X may also serve as an indicator of the reliability of a device. This validates our hypothesis.

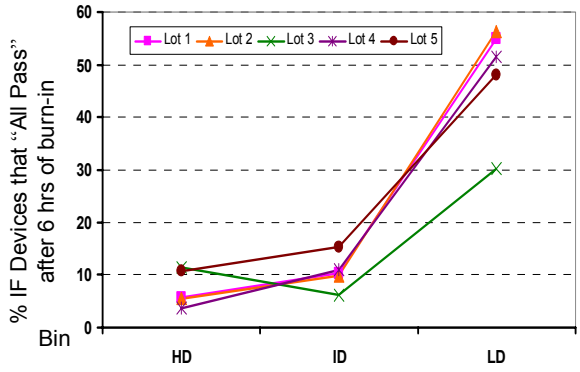

Figure 3. Characteristics of IF devices in bins after 6-hrs of burn-in

We then compare the reliability screening of Delta-IDDQ with X-IDDQ based on these selected IF devices from Lot 1. Only 6% of devices in Bin HD pass all tests after burn-in. This indicates that the Bin HD contains low reliability devices that have high probability of failing burn-in tests. Of the devices that fail Delta-IDDQ test, 18% pass all tests after burn-in. So if devices were to be screened for reliability without undergoing Burn-in, X-IDDQ will screen unreliable devices with higher confidence than Delta-IDDQ.

6. Evaluation of X statistic

In the results presented in Table 2, the z-score values of devices in the different lots were computed using the V matrix obtained using all the 15 IDDQ vectors of devices that passed all the tests (AP), in Lot 1. Now we examine how effective the matrix V from a lot is in binning devices of another lot. Table 4 shows the results when PCs are computed individually for each lot by using its own AP devices.

Table 4. Binning using V from same lot

Lot 2 – 1003 devices						
Bin	**AF**	**AP**	**DF**	**FF**	**SF**	**IF**
HD	240	0	58	3	17	40
ID	7	0	9	1	3	56
LD	6	494	22	1	7	39
Lot 3 – 2368 devices						
HD	330	0	132	2	17	48
ID	12	0	10	2	3	109
LD	17	1779	44	46	21	66
Lot 4 – 2651 devices						
HD	371	0	136	23	28	57
ID	17	3	17	27	7	126
LD	30	1506	55	76	46	35
Lot 5 – 6450 devices						
HD	906	0	350	7	28	158
ID	43	6	58	10	8	344
LD	44	3968	274	83	72	91

Comparing Table 4 with Table 2, no significant change in the characteristic of devices binned is observed. This suggests that the transformation metrics obtained using one lot of devices works very well for other lots. This outcome is advantageous as it eliminates the need of computing PCs each lot. V can be pre-computed based on an initial set of devices for use with fast on-line binning.

7. Conclusion and future work

X-IDDQ technique extracts the fault related information present in a set of IDDQ measurement into a single statistic X. It allows the identification of outlier devices. The probability of a fault-free device appearing as an outlier in IDDQ domain is extremely low. Thus, with only the IDDQ measurements, a significant fraction of faulty devices that fail stuck-at, delay and functional tests can be isolated. An overwhelming majority of the devices in the High Defect Bin fail all or a combination of stuck-at, functional or delay tests. The remaining devices in the bin have abnormal IDDQ profiles, and have a high

burn-in failure rate. These devices need not be tested further. The Intermediate Defect Bin contains a smaller fraction of devices from the lot that fail some or the other tests. Applying additional tests to these devices will help screen the defects better. Majority of devices in LD bin pass all the tests and are better in terms of reliability. Further, the devices in this that fail traditional IDDQ test methods have a significantly lower burnout rate compared to a typical device. Therefore, reduced additional testing effort is needed for these devices.

Thus a test strategy can be proposed based on X-IDDQ in which all the devices undergoing IDDQ testing initially are later subjected to X-IDDQ after a PCA based transformation of IDDQ measurements. Significant savings in test time and reduced test costs are achieved because of removing devices in High Defect bin from further testing. Since the burn-in failure rate is significantly less for parts in the Low Defect bin and high for devices in the High Defect bin, X-IDDQ offers a method of eliminating burn-in for those devices.

Sometimes the concept of IDDQ testing at the beginning of a test suite, to rapidly screen parts that would fail other tests, is not preferred. This is because it masks valuable failure information that is needed for yield improvement. In such situations, X-IDDQ could be implemented as a more effective outlier screen as the last test in a suite rather than the first.

Note that the scheme used for identifying bin boundaries in this study is a very straightforward technique. It is likely that additional research will yield a technique that may result in an even better outcome. The proposed technique can incorporate additional analog parameters such as F_{max}, Min V_{DD}, etc. along with IDDQ measurements, and outlier detection using such a comprehensive set of measurements is likely to further enhance testing and binning process. This technique can potentially be extended to testing of analog devices as well.

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