

An Outlier Detection Based Approach for PCB Testing

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Abstract

Capacitive Leadframe testing is an effective approach for detecting faults in printed circuit boards. Capacitance measurements, however, are affected by mechanical variations during testing and by tolerances of electrical parameters of components, making it difficult to use threshold based techniques for defect detection. A novel approach is presented for identifying boards that are likely to be outliers. Based on Principal Components Analysis (PCA), this approach treats the set of capacitance measurements of individual connectors or sockets in a holistic manner to overcome the measurement and component parameter variations inherent in test data. The effectiveness of the method is evaluated using measurements on three different boards. Enhancements to the technique to increase the resolution of the method are presented and evaluated.

Keywords: Board testing, capacitive open testing

1. Introduction

The Capacitive Leadframe Testing technique (known as TestJet® or its enhanced version VTEP® in industry) is an effective method used in printed circuit board testing [1]. With this technique, open pins can be detected without having to power the tested board by measuring the capacitance between a pin and a tester sense plate.

The TestJet technique tests for open pins in connectors and sockets on boards, using the capacitance formed between a device pin and a suspended sensing plate [1]. During TestJet test, the pin under test is connected to an AC signal source while all other pins are connected to ground as shown in Figure 1. An open pin changes the measured capacitance to an abnormal one. In TestJet test results, a normal test reading means that there is no defect, and a low test reading is an indication that the signal pin itself is open [2][3]. However, in large scale manufacturing, parameter variations from component to component and board to board affect the lead capacitance values. Furthermore, the variation from test fixture to test fixture, and the variation from test system to test system affect the measurements and their accuracy. A good board tested in

one environment may change to be a 'bad' one in another test environment. Sometimes a test may have to have a new limit set generated when executed in a new test environment. With evolving technologies, and consequently, the increasing densities of components and boards, the margins available for deciding among faulty and fault-free devices are shrinking. This limits the ability of TestJet method to detect defects.

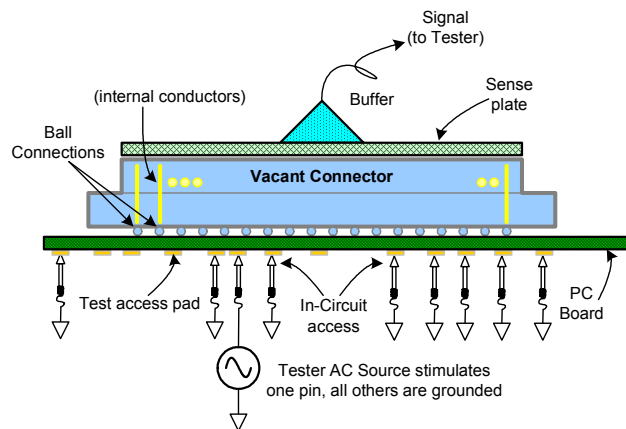


Figure 1 The 'test jet' structure

Threshold Setting is used currently with capacitive testing to differentiate the normal values from the abnormal capacitance values. The shrinking size of the features and the resulting lower capacitance of signal pins make it more and more challenging to set such a threshold value. Relative thresholds based on standard deviation are also made ineffective by these factors. Non-optimal threshold settings can result in higher false fails or false passes. The challenge is further compounded due to the fact that each pin tested has a threshold that is different from others, yet often correlated to them. Furthermore, mechanical parameters such as spacing between the plate and the connector/device vary from one mounting on the tester to another. Similarly, the capacitance value corresponding to a pin may vary from board to board due to the fact that components are from different vendors. These and other factors combine to make the selection of appropriate thresholds a challenging task.

A printed circuit board, also referred to as a board, is a unique assembly that contains many devices. We use data

from a set of three boards with connectors for DDR2 RAM to evaluate our scheme. A device (such as a connector or socket) is unique item with a collection of numbered pins, which are subject to testing with the exception of VDD and ground pins. Multiple devices with unique names may exist on a single board. For example, j3 and j24 are standard connectors used in DDR2 RAM boards.

In this paper we present a novel method for PCB testing, based on Principal Components Analysis (PCA), to improve the efficiency and decrease the potential false classification rate of the TestJet technique. It changes the testing paradigm from one that compares values against fixed thresholds to one that detects outliers. Thus, if the majority of the boards are fault-free, the outliers, which by definition are significantly different from the rest of the boards, are likely to be abnormal or even defective. The method relies on an ensemble of measurements, allowing it to identify correlations among pin capacitances. Thus it can adapt to board-to-board, device-to-device, fixture-to-fixture, and test system to test system variations more effectively than traditional techniques.

PCA based outlier detection has been investigated and found effective for testing of ICs in [4][5][6][7]. It is a successful statistical test technique for the detection of faulty ICs whenever analog test measurements are involved, e.g., IDDQ, delay, power etc. With PCBs however, the defect characteristics of faults and their manifestation in measured values are significantly different from those with ICs. For example, in PCBs, the effects of defects are more localized, and the tests are able to capture spatial distributions. These spatial distributions indicate the recognition of correlations among measurements of adjacent pins. The concept of test pattern associated with ICs is not applicable for PCB capacitance measurements. Furthermore, the measured values can vary over a wide range from pin to pin in good boards and connectors.

This paper presents and evaluates a PCA based outlier detection scheme for PCBs, where the set of measurements per device or a connector is used in a holistic manner to detect the outliers. An extension of this global method is presented in which the analysis is carried out separately for small subsets (windows) of pins. Latter scheme, the localized method, exhibits better sensitivity for connector testing due to the fact that the effects of an open pin are likely to be limited to a small set of neighboring pins. Furthermore, it makes the identification of the specific pin affected easier as the abnormal pin is localized to within the window size.

Section 2 outlines the PCB based outlier detection scheme. The TestJet measurement data used for evaluation of the effectiveness of the scheme is described in Section 3. Section 4 evaluates the proposed scheme, and compares it with the traditional threshold-based approach, where the threshold is set as a multiple of standard deviation of measurements. In Section 4, we also present and evaluate a

modification to the basic strategy, to enhance its sensitivity. Window size selection is discussed in Section 5. Conclusions and future research are presented in Section 6.

2. PCA Based Outlier Detection

Let the $M_{m \times n}$ be the matrix of capacitance measurements, where m is the number of boards, each with n measurements corresponding to the n tested pins. Let M_c be the centered matrix where mean value of its column is subtracted from each element. The mean value of the column is the “measured capacitance of a pin averaged over all boards”.

Singular Value Decomposition (SVD) technique is used to compute U , S , V such that $M_c = USV^T$, where the columns of U and V are called singular vectors, and S is the diagonal matrix containing the singular values [8][9][10][11].

The PC score or Z-score matrix $Z_{m \times n}$ is given by,

$$Z = M_c V \quad (1)$$

Each board is now characterized by n PC scores or Z scores, given by the corresponding row of Z . The first coordinate (called the first principal component) accounts for the largest variance projected from data, then the second one, and so on

In SVD, algorithm forces the first component to go through origin while maximizing the variance projected. Use of centered matrix ensures that the first coordinate is not forced to pass through the origin, and thus can catch the real maximum projected variance from the data.

With a centered data matrix, a second method may be employed to compute the principal components. It involves the computation of the covariance matrix C of the centered matrix: $C = M_c M_c^T$, followed by Eigen Value Decomposition (EVD) to get the score matrix [5]. However, Compared to SVD, EVD sometimes causes information loss. In contrast SVD is the more robust, reliable, and precise method with no need to compute the input covariance matrix. SVD is well known for its convergence and stability property, and works well even for problems with ill conditioned matrices [11].

To detect the outliers, i.e., boards or connectors with test measurement patterns that are significantly different from the rest of the boards or connectors, a distance measure is used. Since the variance of the first and last few PCs vectors contain different information, the first few PCs and last few PCs can detect different types of outliers. Different test statistics such as d_{1i} , d_{2i} , d_{3i} and d_{4i} have been defined which also can be applied for detecting different type outliers [8]. We evaluated the PCB test data for a variety of connectors and boards, and compared the results based on different distance metrics. The test statistic d_{1i}

with the most significant PCs was found to be the most effective and stable one for PCB outlier analysis. Thus we use the d_{li} test statistic formally defined as:

$$d_{li} = \sqrt{\sum_{k \in E} z_{ik}^2} \quad (2)$$

where, z_{ik} is the value of the k^{th} PC for the i^{th} board, and E is a subset of PCs. E is typically selected to be the most significant or the least significant set of PCs [8]. For testing of PCBs, we use the above procedures to calculate the d_{li} value (called d_l below) for each board run. Then we sort the runs with respect to the d_l , and plot the cumulative distribution function (CDF) of d_l , i.e., the d_l value on the horizontal axis and the percentage of devices with a value less than the given d_l on the vertical axis. The outliers are clearly identifiable on the right side of the plot, and typically are separated from other devices by a clear margin.

The basic concept for PCA based test technique was described above. We use two different schemes based on the same technique for testing the PCBs. First, with the *global method*, we use the entire data set for the board to identify outliers. Then calculation concluding formula (1) and (2) is applied to the whole measurement matrix. This method takes into account the variations such as tester to tester variation or fixture to fixture variation more effectively as effect of such variations manifest over the entire set of measurements. However, a weakness of this method is the fact that an open in one pin influences on the capacitance values of only few other pins in its neighborhood. Thus the overall effect on the test statistic is like to be somewhat smaller, as the analysis is based on the dataset for the entire set of pins.

Therefore in *localized method*, we apply the outlier detection scheme on a small window of pins at a time. The original measurement matrix M was first sorted according to the pin number in relative physical layout area. Then the matrix is vertically separated into different small matrixes (test window), where the similar calculation in global analysis is applied.

To cover the entire connector or the set of pins, the test is performed by carrying out test in each window to cover the entire set of pins, one window at a time. Thus we have two options, overlapping windows or non-overlapping windows. In the next section, we investigate the effectiveness of these techniques.

3. Test Data

The measurements forming the test data set correspond to connectors residing on boards tested in a working production line using an Agilent 3070 tester running VTEP. For each connector on the board, all but grounded/VDD pins were tested and capacitance measurements obtained. A board may be tested more than once, so there can be a data record (termed *board run*) for each test of the same dataset (and each of its devices). We use three sets of measurements, as indicated in Table 1.

Data_j24 corresponds to a j24 connector in 47 unique tested boards. Since some of the boards were tested multiple times for variation comparison, there are a total of 83 board runs in this data set. Figure 2 illustrates this test data set. Data_j3 is from a j3 connector (DDR2 RAM) and corresponds to 6 unique boards. A more comprehensive set, Data_D1, includes 17 unique boards with 20 sets of board runs. Each of the board in Data_D1 includes eight connectors: j7, j10, j13, j16, j41, j45, j47 and j50. The multiple connectors lead to over 1000 pins tested per board.

Visual inspection of Figure 2, based on test data from j24 connectors, identifies certain clear outliers, namely the boardrun numbers 17, 18, 19, 20, 21, 22. Of course there are other outlier board runs besides the six above that are harder to identify by a visual inspection. Test results for pins 210 to 240 (the right part of plot) have a significantly higher variation compared to the others. A close inspection of the plots for different boards shows strong fluctuations in measurements with values that are far different from each other.

Table 1 Data sets and the number of tested pins included

Data Name	Unique Board	Board Runs	Tested Pins
Data_j24	47	83	145
Data_j3	6	6	142
Data_D1	17	20	1053

4. Test Results

In this section we present outlier detection results for PCBs with the two test methods presented in Section 2. First, with the *global method*, we use the entire data set for the board to identify outliers. In *localized method*, we apply the outlier detection scheme on a small window of pins at a time, and repeat this over multiple windows to cover the entire set of pins.

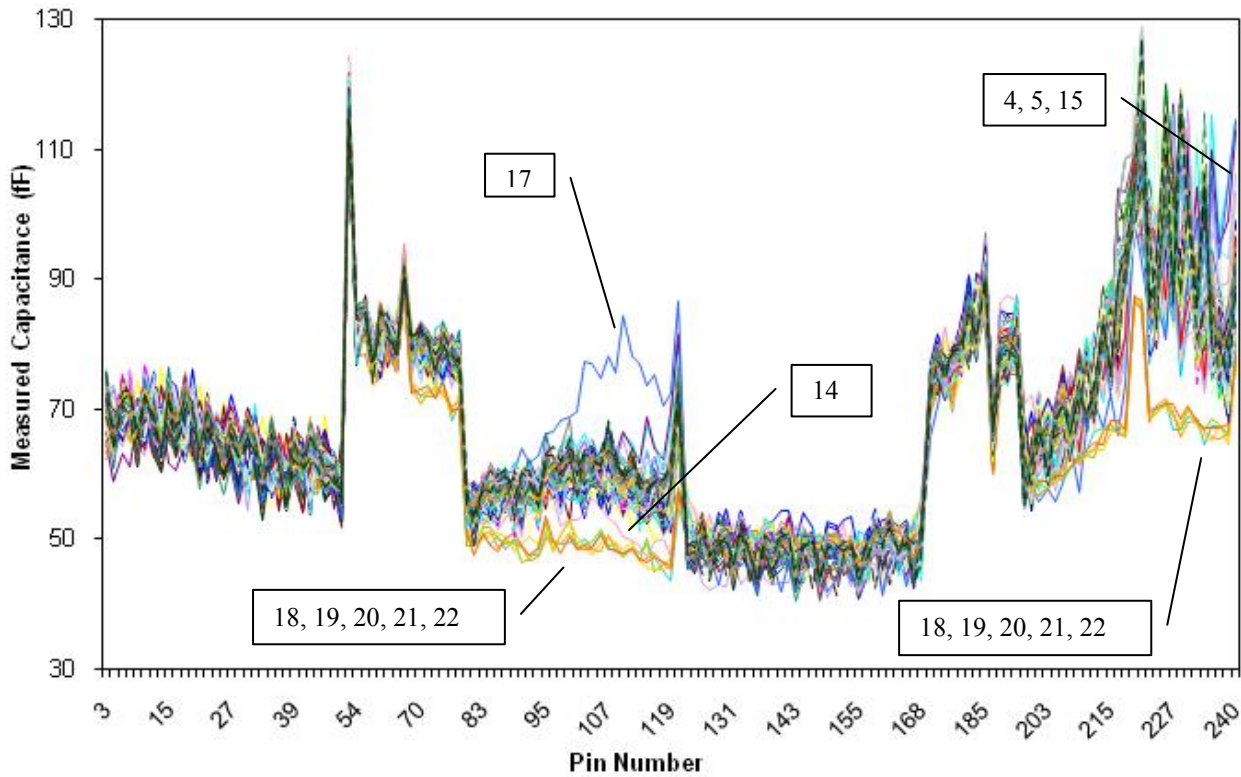


Figure 2 Capacitance vs. pin number for Data_j24

4.1 Global Method

First we calculate the d_i values for each of the boards in the data set using Equation (2), selecting the first 5 PCs. Extensive experimentation with data presented here and other data sets indicates that the more significant PCs provide better outcomes in PCB testing. Figure 3 shows the variance of different principal components, which indicates that the first 15 principle components carry almost all the information about the data set. This is almost always the case irrespective of the type of data set. However, depending on the data type or the problem domain, the more significant or less significant components are more effective in detection outliers. In case of IDDQ data, for example, less significant components are more useful in detecting the outliers [4]. But with PCB test data, the more significant components appear to be more useful for detection of outliers. Figure 4 shows the CDF plot for d_i for all of the board runs in Data_j24. To avoid clutter, we have labeled only a select set of board runs in the CDF. However, points corresponding to other board runs are present in the plot, and the sequence of sorted board run numbers provided with the figure can be used to identify the position of a particular board run on the CDF plot. The plot of the CDF shown in Figure 4 clearly identifies the outlier board runs, which appear at the right extreme separated from the remaining board runs.

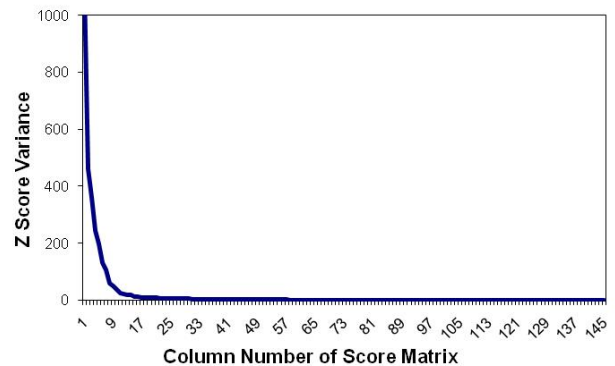
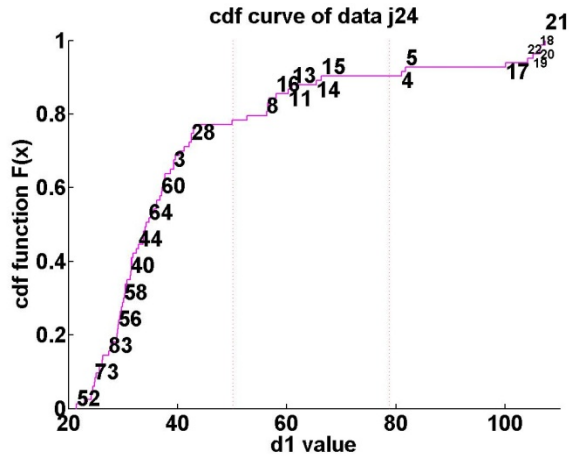


Figure 3 PC vector variance plot to Data_j24

Board runs 17, 18, 19, 20, 21 and 22 all clearly stand out at the high end of CDF curve where they indicate much larger d_i values than the other board runs. The runs 18, 19, 20, 21 and 22 are five repeated tests of the same board. However, as can be seen from Figure 2, while the general pattern remains the same, the measurement variation among different runs is often comparable to measurements among subsets of different boards. These six runs would be identified as outliers by manual inspection of data. In the plot, the six board runs show a clear break from others which means that they are far different from others based

on the holistic PCA analysis. With the first few PCs used, the outliers detected in the d_i value of CDF plot match the observations from the raw data plot. With another clear break at the high tail of CDF plot, some other board runs like 5, 4 are also identified as possible outliers depending on the degree of filtering desired. A careful inspection of the right end of Figure 2 indicates these two board runs to show abnormal value.



Board run numbers on CDF plot from left to right:

52,51,50,53,49,32,73,24,48,25,74,72,83,71,57,47,1,42,56,70,6,68,38,37,58,43,59,41,39,55,40,2,23,78,33,35,44,69,79,54,7,5,36,64,80,76,31,77,65,60,29,81,63,61,62,3,67,66,82,27,45,2,8,46,26,30,34,12,8,7,10,9,16,11,13,14,15,4,5,17,22,19,18,20,21

Figure 4 CDF plot of d_1 for Data_j24

In contrast to Data_j24, which is for a board with a single connector, the Data_D1 with 20 board runs is for a board with 8 tested connectors, which leads to over one thousand tested pins per board. Compared with measurement matrix of data_j24 of dimension 145×83 , the dimension of matrix of Data_D1 is 1053×20 . Manual inspections shows that the boards 8, 9 and 10 show unusual measurements on some of the 1053 pins, which make them clearly different from other boards. In the CDF plot of Figure 5, d_i CDF plot clearly shows the three outliers at the right end, which coincide the three board runs with abnormal measurements. So, the d_i values with the first few PCs can detect the clear outlier board runs. This technique can effectively filter the abnormal board runs.

In cases where the number of measured pins per board is quite large, such as in this case, it is difficult to identify defects that affect only the measurements on one or small subset of pins by a relatively small magnitude. For such cases, a more sensitive scheme is needed that takes into account local perturbations, i.e., those limited to a very few neighboring pins.

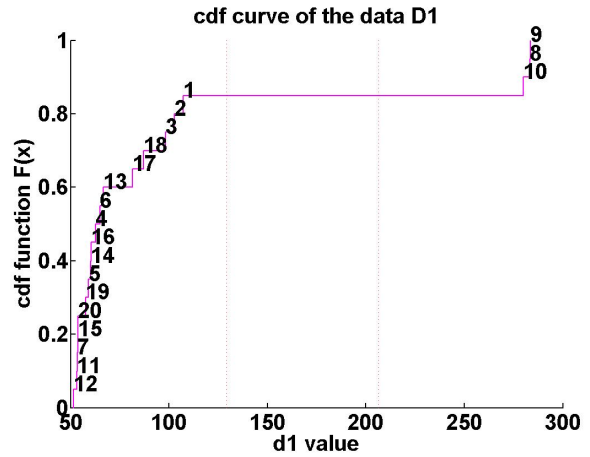


Figure 5 CDF plot of d_i for Data_D1

4.2 Localized Method

As the open of one pin influences the capacitances of only a few neighboring pins, we propose the use of a window of neighboring pins for outlier detection. The method requires the test data to be sorted according to the physical order of pins on the connector. The union of outliers from different windows is considered to be the set of outliers. This section also considers the selection of the window size as well as use of overlapping windows to further enhance the scheme.

Localized method as discussed above may not be applicable to PCA based outlier detection schemes for other test problems such as IDDQ [4][5], when the effect of faults cannot be localized to a set of measurements. With PCBs, the physical adjacency among the pins is known and the localized analysis method produces a significant increase in sensitivity as illustrated below. Furthermore, it helps isolate the location of the outlier pins to within a small set, resulting in significant saving in the time required for subsequent board inspection and repair.

With the localized scheme, to locate the outlier in Data_j24, all of the tested results are first sorted in the same order as the physical layout of the connector. Ten test windows of 24 pins each were selected equally dividing the 240 pins as shown in Figure 6, note that some of the pins being supply or ground pins are not involved in capacitance measurements. Figure 7 is a plot of measured data, sorted as described. PCA based d_i evaluation is applied to each of the 10 test windows individually. The CDF plots for windows 1 and 10 are shown in Figure 8. It is seen that the different connectors are very similar to each other based on window 1. In window 10, there are clear outliers. Figure 9 plots the maximum d_i value for different windows. Outliers are observed in the last three windows, which clearly indicated breaks in the CDF. This is also evident from the wide range of d_i values in windows 8 to 10 in Figure 9.

In fact, these windows correspond to the 72 pins at the right end of the j24, shown in Figure 6. There is also the possibility that the tester introduced errors such as those due to misalignment of the sense plate. Retesting boards on a different fixture can resolve such issues.

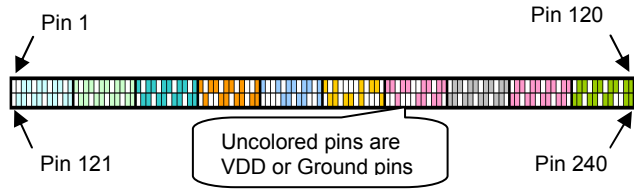


Figure 6 Test window division on j24 connector

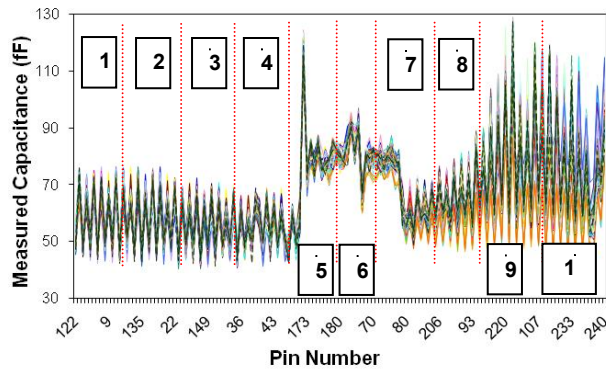


Figure 7 Capacitance vs. position (pin no is sorted per physical layout) and the 10 test windows for Data_j24

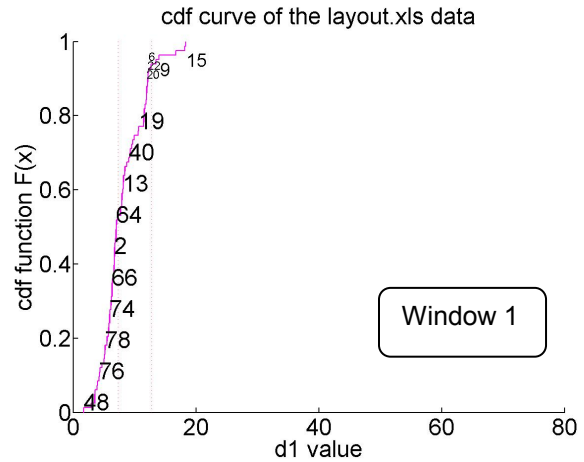
4.3 Analysis with Overlapping Windows

In the previous case, there was no overlap among the different windows used for evaluation. Thus it fails to take into account the impact of a fault on the boundary of one of the windows on the pins in the next window. Thus, another option is to use overlapping windows for the evaluation.

Figure 10 uses test window such that each of them includes the adjacent halves of the two test windows of Figure 9. For example, the test window 1 in Figure 9 includes pins {122, 3, 123, 4, 125, 6, 126, 7, 128, 9, 129, 10, 131, 12 and 132}; the test window 2 in Figure 9 includes pins {13, 134, 15, 135, 16, 137, 18, 138, 19, 140, 21, 141, 22, 143, 24 and 144}. The overlapping test windows in Figure 10 are named after the two test windows in Figure 9 they overlap. For example, window 1-2 in Figure 10 includes the second half of original window 1 and first half of original window 2 which are thus {128, 9, 129, 10, 131, 12, 132, 13, 134, 15, 135, 16, 137, 18, 138}. Note that the unlisted pins are VDD or grounded pins.

The plots of the maximum d_i value in both Figure 9 and Figure 10 are similar. In this case, there is no fault that is influencing measurements on pins of adjacent non-overlapping window. However, in general, such cases

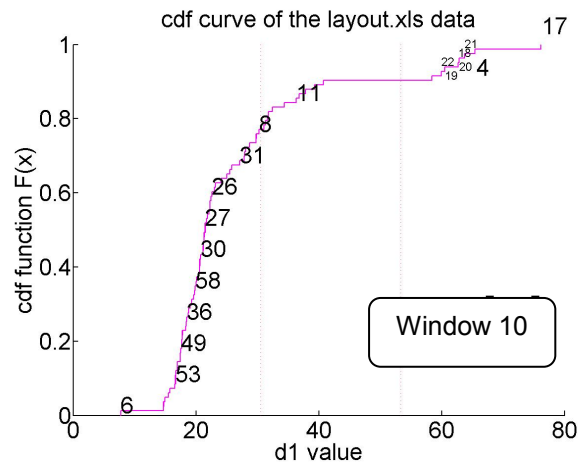
cannot be ruled out. The overlapping test window can be used to identify the location of outlier pins more finely by combining the analysis using both original and overlapped windows.



Board run numbers on CDF plot from left to right:

48,79,77,72,53,81,39,76,73,80,47,51,31,32,78,44,49,75,50,33,56,74,52,68,43,82,61,24,66,1,23,69,25,42,46,2,37,30,35,41,60,45,64,83,71,70,54,4,38,13,62,28,29,7,67,63,40,10,65,26,34,11,55,19,59,27,58,21,17,12,8,18,20,57,22,36,6,3,16,9,14,15,5

(a)



Board run numbers on CDF plot from left to right:

6,52,68,35,71,83,51,53,38,72,37,73,41,57,49,48,55,40,56,29,59,36,47,74,50,39,64,46,58,24,25,54,45,42,43,30,2,1,65,3,61,67,27,6,3,60,62,32,33,28,26,66,70,10,69,44,23,31,34,12,82,78,79,80,8,75,7,77,9,76,16,11,81,14,15,13,5,22,19,18,20,21,4,17

(b)

Figure 8 CDF plot of windows 1 and 10 (a) test window 1 (b) test window 10

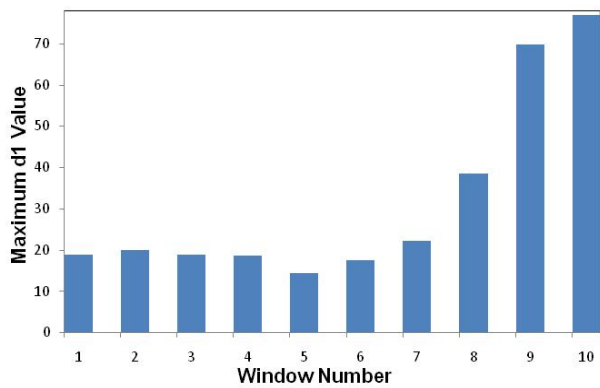


Figure 9 Maximum d_1 value in each windows for connector j24

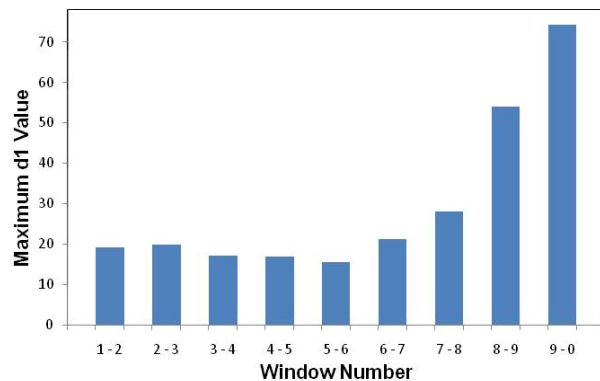


Figure 10 Maximum d_1 value in overlap windows for connector j24

4.4 Comparison of PCA based outlier detection with the standard deviation-based approach

In the traditional approach, the standard deviation of measurement is used to identify the pins considered to be sufficiently different from the others. In the standard deviation method (STDev method), mean and the standard deviation are calculated using the data for all tested pins. The mean value serves as an expected good value. High and low limits are set equal to the average plus/minus $\alpha \times \text{STDev}$, for an appropriately selected α based on the degree of screening desired. For the j24 test data above, the board runs that would be considered as abnormal based on this method, are shown in Table 2 for different values of α .

With the increase of the value of α , fewer and fewer boards are included into the suspected group of boards. Since normally $\alpha \geq 4$ is often used as the threshold, when $\alpha = 4$, the STDev method detects boards 3, 11, 14, 17 and 83 as the abnormal ones. However, the PCA based outlier detection method identifies 18, 19, 20, 21, 22 and 17 as outliers. Note that with the PCA based outlier detection, the decision is significantly more justifiable as the CDF plot clearly separates the outliers. With STDev method, the value of α has to be guessed.

Table 2 The abnormal boards for different α values for Data_j24.

	Abnormal PCB Detected	Boards No.
6	0	
5.5	1	17
5	1	17
4.5	2	14, 17
4	5	3,11,14,17,83
3.5	11	3,4,5,6,8,11,14,15,17,59,83
3	18	3,4,5,6,8,9,11,14,15,16,17,18,19,20,21,51,59,83
2.5	35	3,4,5,6,7,8,9,11,12,13,14,15,16,17,18,19,20,21,22,34,36,47,48,51,53,57,58,59,60,63,68,73,80,81,83

Table 3 Comparison of different outlier detection methods

PCA methods	STD method ($\alpha = 4$)	Expert Selection
18,19,20,21,22,17	3,11,14,17,83	18,19,20,21,22,17

In Table 3, we compare the three methods for data from Data_j24. The last column in Table 3 illustrates outliers detected by manual examination of data. We can see that the outliers detected by the PCA methods match well with those selected by manual inspection of raw data to detect outliers. The STDev method does not treat the different pins fairly; even though two pins may be similar, one may happen to have a wider range due to one or few boards causing a higher deviation for that pin. Figure 11 identifies the specific pins of board runs 3, 17, 83, 14, 11 with STDev method with $\alpha = 4$, with no observable deviation.

More importantly, the standard deviation method does not consider the correlation among the tested pins. In PCBs, an abnormal pin will cause the pins around it show abnormal test values too. The PCA implicitly captures the correlation among different pins for the final result.

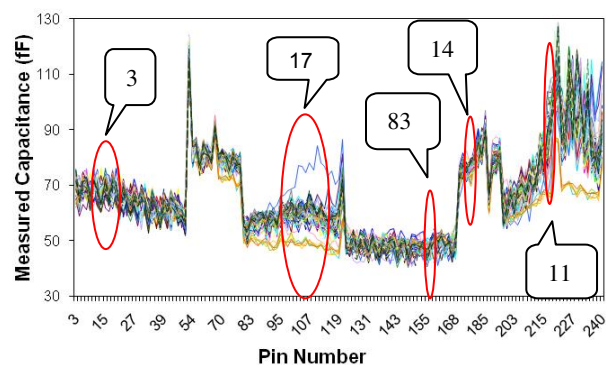


Figure 11 Position of the outliers of Data_j24 on the connector.

4.5 Comparison of global and localized methods

The localized method detects outliers based on the evaluation of one window at a time, and as a result can effectively detect opens in that window. On the other hand,

it can fail to take into account trends of more global nature, such as tester to tester variations, alignment errors, etc. which can be observed when measurements for different devices are compared over a larger window. The global method is more effective in capturing such characteristics. Consider for example TestJet results for Data_j3 as shown in Figure 12, board run 4 shows a clear spike at pin 33. With the localized method, the window 11 with that pin indicates board run 4 as an extreme outlier, i.e., one that is on the right end of the CDF plot separated from others by a significant gap. With the global method, board run 4 doesn't appear as an extreme outlier since all other measures of the connector are within the range of variation of most of the boards. The localized method can work with a relatively few devices, while the global method requires measurements for a relatively larger number of devices. Figure 13 shows the range of d_1 values observed for Data_j3. The larger the range of d_1 , the more likely there are outliers in that window. The outliers can be clearly identified using the corresponding CDF plot.

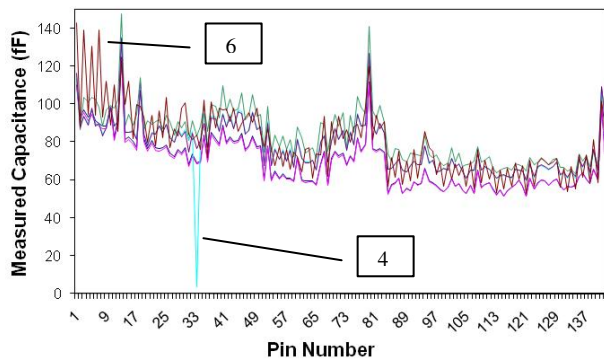


Figure 12 Capacitance vs. pin number for connector j3

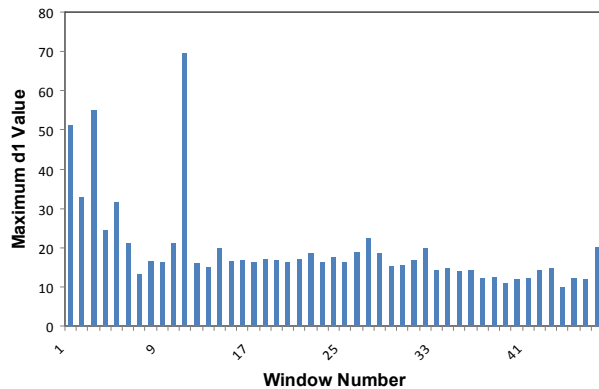


Figure 13 Maximum d_1 value in each window for connector j3

Figure 14 shows the CDF plot of the Data_j3. As can be seen, board run 4 does not produce an extreme d_1 value. After the localized analysis, there are totally five test windows that have a d_1 range higher than 30. Figure 13 identifies these windows, i.e., windows 1, 3, 4, 5, and 11.

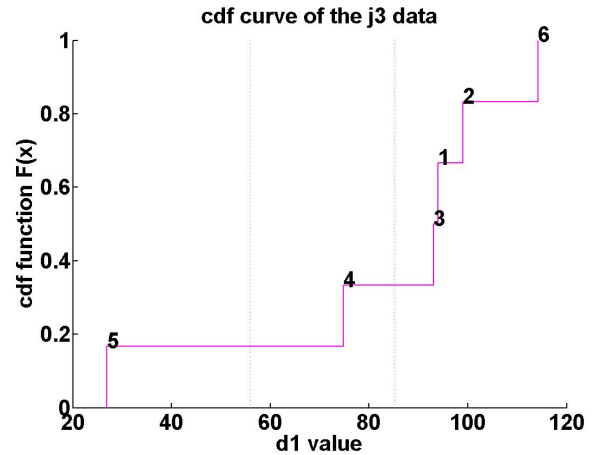


Figure 14 Global analysis of Data_j3

The d_1 value distribution in these five windows is shown in Figure 15. Board run 4 shows an extreme value only in window 11; the other 4 test windows all contain very low d_1 values. Figure 16 shows the CDF plot of test window 11, which gives board run 4 very high d_1 value separating it clearly from the others.

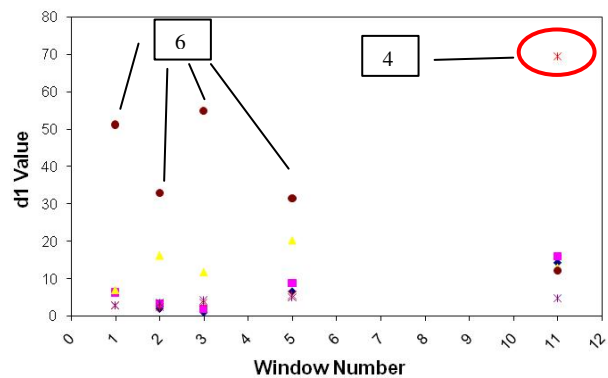


Figure 15 d_1 value distribution in the 5 test windows for Data_j3

Comparing the plots for both the global and localized methods, following observation can be made. Board run 4 does not show high d_1 value in the global analysis. However it shows one very high d_1 value in test window 11. From the overall data viewpoint, board run 4 is one that is very close to the normal range of measurement values for the set of boards; this can also be seen from the measurements plot of board run 4, where except for a single spike, other measurements are well within normal range of variation. A board run that does not show high d_1 value in the overall analysis but appears as an outlier in one or two of the test windows must contain spike signals.

The global method can effectively catch the obtuse outliers like board run 6 in Figure 12. Here the measurements for a group of pins are outside the norm, but each one deviates only slightly from the norm (see Figure 14). The localized method can catch outliers with one or few sharp peaks, such as board run 4. The advantages of the two methods

can be combined by a test technique for connectors by using both global and local analysis and then taking the union of outliers.

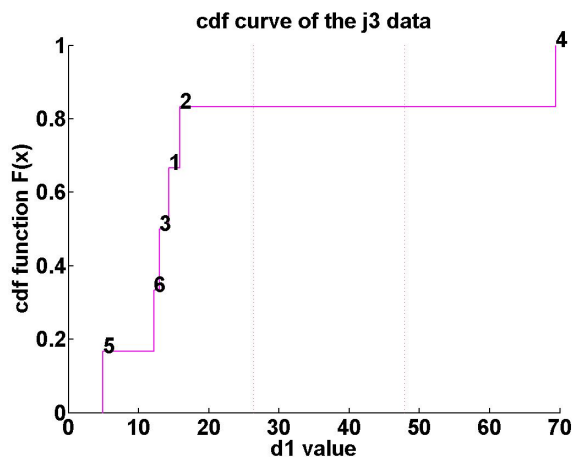


Figure 16 Analysis of test window 11 in Data_j3

4.6 Size of Test Window

The global and localized methods can be considered to be two instances of the same method, where the global method corresponds to a window that contains all the pins. Thus the notion of an optimal window size arises; however optimality is likely to depend on attributes of the dataset. A large window size will make the analysis less sensitive for detection of the precise location of the outliers. It can also cause the problem of peak detection errors mentioned earlier. A large window size can also miss outliers that manifest only on one or very few pins, especially when the total number of pins is large. However, when a test window is too small, it may not be sensitive to the spatial correlation among the measurements. It would also take a lot of computation time to identify the outlier devices.

A preliminary analysis was done to see the impact of window size variation using data for Data_j24. To identify a good criteria for the selection of window size, we use a metric, the maximum value minus the median value for different window sizes. A larger difference, indicates a higher variation in the test window. For example, in Figure 13 the highest d_1 value is the one corresponding to window 11, minus the median d_1 value of all test windows to set the criteria. The larger the difference the clearer the peaks in the test window.

Figure 17 shows the test result of Data_j24, for window sizes varied from 2 to 47. As can be seen, the difference of maximum and median d_1 values increase with the increase of test window size. But no clear increase is seen beyond a window size of 26. However, when the window size is too large, there may only be two or three windows, which will decrease the resolution.

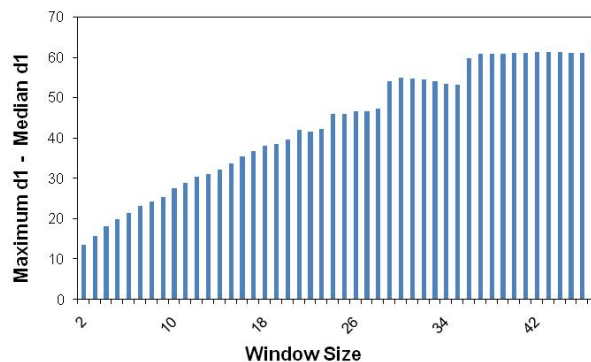


Figure 17 Difference of maximum and median d_1 vs. window size of Data_j24

5. Summary and Future Work

PCA based techniques have been examined for automated identification of outlier printed circuit boards which can potentially be used to identify faulty or marginal boards. We have identified the test statistic d_1 with the most significant principal components, to be the most robust in detecting the outliers in PCBs. The idea of localized analysis, which uses smaller test window, is introduced and analyzed. It can increase test resolution, and can assist in the location of some outliers. Since both the global and localized analysis have some trade-offs in face of some outliers, they can be combined to filter the outliers. Global analysis is able to identify the trends affecting a large fraction of measurements. The proposed PCA based approach has been compared with traditional standard deviation-based approach for identifying outliers. The PCA based approach significantly outperforms this traditional approach. We have found that PCA based approach preserves some of the benefits of examining raw data.

We are investigating techniques to enhance the effectiveness of the outlier detection, and related computational issues for on-line testing. We are also conducting research on the effects of common mechanical variations in sense plate mechanism to see what these effects may be and whether PCA can identify these variations systematically. These variations (such as shifted plates, or plates with a tilt from side to side or variation in air gaps between plate and device) will cause measurement variations that are not indicative of actual defects. We believe they can be filtered out during the diagnostic process. Also under investigation are techniques to diagnose faults based on experimental data from different circuit boards. In future we also plan to investigate the data variation caused by use of different testers; influence of measurement errors introduced by mechanical and electrical tolerances. The resulting techniques would be used to minimize the probability of good board being identified as marginal or bad even when higher board densities reduce the available resolution.

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