

## Coalescing Logistics (Again)

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### Rule

- When building the interference graph, do NOT make virtual registers interfere due to copies.
- If the virtual registers s1 and s2 do not interfere and there is a copy statement  $s1 = s2$  then s1 and s2 can be coalesced.
- Example

```
a = t + u
...
b = a
c = a
...
x = b + w
z = c + y
```

Before Coalescing

```
ab = t + u
...
c = ab
...
x = ab + w
z = c + y
```

After Coalescing

## Architectures with Callee and Caller Registers

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### Alpha

- 7 callee-saved out of 32 registers

### MIPS

- caller-saved: \$t0-\$t9, \$a0-\$a3, \$v0-\$v1
- callee-saved: \$s0-\$s7, \$ra

### PPC

- 18 callee-saved
- 14 caller-saved

### StarCore EABI

- 4 callee-saved
- 28 caller-saved