Fault Tolerant Computing
CS 530
Fault Modeling

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Objectives

• The number of potential defects in a unit under test is extremely large.
• A fault-model presumes that most of the defects can be described by a well defined faults (as given later in this Lecture Notes).
• Here we primarily focus on hardware, however there is something analogous in software (“test coverage”).
Fault Modeling

• Why fault modeling?
• **Stuck-at 0/1 fault model**
• The **single fault assumption**
• Bridging and delay faults
• MOS transistors and CMOS
• **Switch-level fault model**
  – Stuck-on/open
  – Shorts and IDDQ
Fault Modeling

• **Fault Model**: a set of assumed faults in a system such that testing for them will test for most faults of a specific class.

• Used for **test generation**, **fault simulation** and quality evaluation.

• A fault model hides complexities of actual defects. Infinitely many defects possible.

• Fault Models are based on past knowledge of defect modes and modeling experience.
Common Fault Models

• No model: test exhaustively
• Hardware fault models:
  − Gate level:
    • stuck-at 0/1: most common
    • bridging faults
    • delay faults
  − Transistor level: stuck on/open faults
    bridging faults
  − Functional fault models
• Software fault models?
  − No formal fault model, but the software test coverage concept is closely related.

Exhaustive testing: Applying all possible combinations
Failure mechanisms in hardware

• **Temporary**: sensitivity to charged particles etc.

• **Permanent**
  - **Opens**: broken connection, also near-opens
  - **Shorts**: unwanted connection, also near shorts
  - Can be seen in magnified chip photos
  - Others

• **Imperfect devices**
  - Analog impairments like excessive delays
Stuck-at 0/1 Model

• Classical model, well developed results/methods
  – Many opens and shorts result in a node getting stuck-at a 0 or 1.
• May not describe some defects in today’s VLSI.
  – still a nice way of structural “probing”. Covering all stuck-at 0/1 will result in covering a large fraction of all faults.
• Model: any one or more of these may be stuck at 0 or 1: *a gate input, a gate output, a primary input*.
• Justification: many lower level defects can be shown to have an equivalent effect.

Common abbreviations: s-a-0, s-a-1
What is a “test”? 

- **A test for a specific fault** is an input combination which results in different outputs for the normal and faulty circuits.
  - Application of a test will reveal the presence or absence of that fault, by observation of the output.
- **For a combinational circuit, a test is called a test vector or a test pattern.**
- **A set of tests is called a test set.**
Stuck-at 0/1 Example

Normal function: \( Z = x_1x_2 + x_2x_3 \)

Faulty Function when a fault is present:
- \( x_2 \) s-a-1 \( \Rightarrow \) \( z = x_1 + x_3 \)
- \( a \) s-a-1 \( \Rightarrow \) \( z = x_1 + x_2x_3 \)
- \( b \) s-a-1 \( \Rightarrow \) \( z = x_1x_2 + x_3 \)
- \( c \) s-a-1 \( \Rightarrow \) \( z = 1 \)
- \( z \) s-a-1 \( \Rightarrow \) \( z = 1 \)

Note that a s-a-0 and \( X_2 \) s-a-0 have different impact.

Example: Find a test vector for \( x_2 \) s-a-1:
Input = \( (x_1, x_2, x_3) = (0, 0, 1) \) Output = 0 normally
1 if faulty
Single Fault Assumption

• Assumption: only one fault is present at a time.
• Significantly reduces complexity.
• Good for fault detection: complete single stuck test set will detect almost all multiple faults.
• Not good for fault location.
• A Multiple fault is a simultaneous presence of several single faults.
• How many multiple faults in a unit?
  − Assume k lines
  − 3 states per line: normal, s-a-0, s-a-1
  − Total $3^k-1$ faulty situations! (For k=1000, total $1.3 \times 10^{477}$)

One among $3^k$ situations is a normal unit.
Delay Faults

• Some defects can cause a gate to respond after an excessive propagation delay.
• As a result some chips will not work at the intended clock frequency, but may work at a lower frequency (i.e. slower speed).
• Delay faults are quite common and thus all chips must undergo testing for potential delay faults.
Bridging (Short) Fault Model

- Model: Two lines can get shorted (bridged)
- Common assumption: only *nearby* lines can be bridged.
- Impact of a short can depend on the technology and transistor dimensions. Sometimes a 0 dominates over a 1 causing both bridged lines to become 0. Sometimes a 1 may dominate.
Transistor Level Faults

• A digital circuit has two power supply terminals: High (often called $VDD$) and Low (often called ground).

• A transistor is a switch that either on (conducts current) or open.

• Output of a gate is High (1), when the output is connected to High terminal through the transistor assembly. Similarly the output is Low (0) when it gets connected to Low terminals.
Transistor-level faults: Impact

Shorts or opens in the transistor assembly can cause these behaviors:

• Output cannot become 1
• Output cannot become 0
• Output behaves as if one of the inputs was always 1 (or 0), regardless of actual value of the input.
• If an output gets connected to both High and Low supply terminals at the same time, it causes shorting between them, causing a very high current to flow. Current-based testing is often called IDDQ testing.
References

- W.K. Al-Assadi, Y.K. Malaiya, A.P. Jayasumana,
Special Interest Slides

- The rest of the slides in this Lecture Notes are specialized. Skip them, unless you intend to work in hardware testing field.
MOS Transistors

N-channel

\[ 0 = \text{open} \quad \quad 1 = \text{closed} \]

P-channel

\[ 0 = \text{closed} \quad \quad 1 = \text{open} \]
CMOS NOR Gate

A=1
B=0

\( V_{DD} = H \)

on
off

Output=0

on
off

Gnd=L

verifying

1
0
0

0

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Switch-level Fault Model (1)

- Model: A transistor may be
  - stuck-open
  - Stuck-on

- PA stuck-open: output effectively s-a-0
- NA stuck-open: To sensitize output (A,B)=(1,0)
  - Normal output: 0
  - Faulty output: high imp: previous value: sequential behavior!
- Needed test-pair
- T1 (0,0) output= 1 (initialize)
- T2 (1,0)
  - 0 normal test
  - 1 if faulty
Switch-level Fault Model (2): Stuck-ON

- Assume PA is stuck-ON
- \((A,B)=(1,0) \Rightarrow\) normal out=0, faulty out=?
- Depends on relative resistances (dimensions etc)
- Low resistance between \(V_{DD}\) and Gnd: very high supply current \(I_{DDQ}\)
Shorts and IDDQ

• Logical value can not be predicted in general.
• Very high supply current ($I_{DDQ}$)
• Generally $I_{DDQ}$-based testing is very effective for detecting some defects.
Impact of Bridging Faults

Faulty function with AND bridging:

\[ Z_1 = (x_1 \cdot x_2) + (x_1 \cdot x_2) = x_1 \cdot x_2 \]
\[ Z_2 = (x_1 \cdot x_2) + x_3 \]

Feedback bridging can cause

• Oscillations: odd inversions, sufficient delay
• Settling at intermediate voltage level
Delay Fault Model

- *Excessive path delay* or *gate delay*
- Signals may get sampled before stabilization
- Example: OR gate delay increases from 0.2 to 0.8 ns.

The fault causes the longest path to take 1.2 ns, causing sampling before signal stabilizes.