Schedule : Fall 2017

This is the tentative schedule of Mélange group for the Fall 2017 semester.

Meet time & Place : Wednesdays 10:00 AM - 11:00 AM @ CSB 305

WEEK	DATE	TOPIC	PRESENTER
0	08/23/2017	No Meeting	
1	08/30/2017	AMD Ryzen CPU Zen Cores Architecture	Steve Kommrusch
2	09/06/2017	AMD Ryzen CPU Zen Cores Architecture (Contd...)	Steve Kommrusch
3	09/13/2017	Elevator talks	-
4	09/20/2017	Elevator talks	-
5	09/27/2017	TBD	
6	10/04/2017	TBD	
7	10/11/2017	TBD	
8	10/18/2017	TBD	
9	10/25/2017	TBD	
10	11/01/2017	TBD	
11	11/08/2017	TBD	
12	11/15/2017	TBD	
13	11/22/2017	FALL BREAK	-
14	11/29/2017	TBD	
15	12/06/2017	TBD	
16	12/13/2017	TBD	

Reading Pool

Publications

2017

- Chris Cummins, Pavlos Petoumenos, Zheng Wang, Hugh Leather, Synthesizing benchmarks for predictive modeling, 2017
- Johannes Doerfert, Tobias Grosser, Sebastian Hack, Optimistic Loop Optimization, 2017

2016

- Wenlei Bao, Changwan Hong, Sudheer Chunduri, Sriram Krishnamoorthy, Louis-Noel Pouchet, Fabrice Rastello, P. Sadayappan, Static and Dynamic Frequency Scaling on Multicore CPUs, 2016
- William Ogilvie, Pavlos Petoumenos, Zheng Wang, Hugh Leather, Minimizing the cost of iterative compilation with active learning, 2016

- U. Bondhugula, V. Bandishti, I. Pananilath, Diamond Tiling: Tiling Techniques to Maximize Parallelism for Stencil Computations, 2016
- Audrunas Gruslys, R{ '{e}}mi Munos, Ivo Danihelka, Marc Lanctot, Alex Graves, Memory-Efficient Backpropagation Through Time, 2016
- Daniel J. Milroy, Allison H. Baker, Dorit M. Hammerling, John M. Dennis, Sheri A. Mickelson, Elizabeth R. Jessup, Towards Characterizing the Variability of Statistically Consistent Community Earth System Model Simulations, 2016

2015

- T. Nowatzki, J. Menon, C. H. Ho, K. Sankaralingam, Architectural Simulators Considered Harmful, 2015
- J. D. Garvey, T. S. Abdelrahman, Automatic Performance Tuning of Stencil Computations on GPUs, 2015
- Eric Chung Kalin Ovtcharov, Accelerating Deep Convolutional Neural Networks Using Specialized Hardware, 2015
- Protonu Basu, Mary Hall, Samuel Williams, Brian Van Straalen, Leonid Oliker, Phillip Colella, Compiler-Directed Transformation for Higher-Order Stencils, 2015

2014

- Sharan Chetlur, Cliff Woolley, Philippe Vandermersch, Jonathan Cohen, John Tran, Bryan Catanzaro, Evan Shelhamer, cuDNN: Efficient Primitives for Deep Learning, 2014
- Andrew Putnam, Adrian M. Caulfield, Eric S. Chung, Derek Chiou, Kypros Constantinides, John Demme, Hadi Esmaeilzadeh, Jeremy Fowers, Gopi Prashanth Gopal, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, Joo-Young Kim, Sitaram Lanka, James Larus, Eric Peterson, Simon Pope, Aaron Smith, Jason Thong, Phillip Yi Xiao, Doug Burger, A Reconfigurable Fabric for Accelerating Large-scale Datacenter Services, 2014

2013

- Martin Kong, Richard Veras, Kevin Stock, Franz Franchetti, Louis-No “{e}l Pouchet, P. Sadayappan, When Polyhedral Transformations Meet SIMD Code Generation, 2013
- Louis-Noel Pouchet, Peng Zhang, P. Sadayappan, Jason Cong, Polyhedral-based Data Reuse Optimization for Configurable Computing, 2013

2012

- Vinayaka Bandishti, Irshad Pananilath, Uday Bondhugula, Tiling Stencil Computations to Maximize Parallelism, 2012

2011

- A. Pedram, A. Gerstlauer, R. A. v. d. Geijn, A high-performance, low-power linear algebra core, 2011
- Henry Wong, Vaughn Betz, Jonathan Rose, Comparing FPGA vs. Custom Cmos and the Impact on Processor Microarchitecture, 2011

2010

- J. Ramanujam Sanket Tavarageri, P. Sadayappan, Parametric Tiling of Affine Loop Nests, 2010

2008

- Andrew R. Putnam, Dave Bennett, Eric Dellinger, Jeff Mason, Prasanna Sundararajan, CHiMPS: A High-level Compilation Flow for Hybrid CPU-FPGA Architectures, 2008

2001

- Steven J. Deitz, Bradford L. Chamberlain, Lawrence Snyder, Eliminating Redundancies in Sum-of-product Array Computations, 2001

1994

- J. Cong, Yuzheng Ding, FlowMap: an optimal technology mapping algorithm for delay optimization in lookup-table based FPGA designs, 1994

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