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@inproceedings{Pouchet:2013:PDR:2435264.2435273, author = {Pouchet, Louis-Noel and Zhang, Peng and Sadayappan, P. and Cong, Jason}, title = {Polyhedral-based Data Reuse Optimization for Configurable Computing}, booktitle = {Proceedings of the ACM/SIGDA International Symposium on Field Programmable Gate Arrays}, series = {FPGA '13}, year = {2013}, isbn = {978-1-4503-1887-7}, location = {Monterey, California, USA}, pages = {29-38}, numpages = {10}, url = {<http://doi.acm.org/10.1145/2435264.2435273>}, doi = {10.1145/2435264.2435273}, acmid = {2435273}, publisher = {ACM}, address = {New York, NY, USA}, keywords = {compilation, data reuse, high-level synthesis, program transformations}, }

@article{Kong:2013:PTM:2499370.2462187, author = {Kong, Martin and Veras, Richard and Stock, Kevin and Franchetti, Franz and Pouchet, Louis-Noel and Sadayappan, P.}, title = {When Polyhedral Transformations Meet SIMD Code Generation}, journal = {SIGPLAN Not.}, issue_date = {June 2013}, volume = {48}, number = {6}, month = jun, year = {2013}, issn = {0362-1340}, pages = {127-138}, numpages = {12}, url = {<http://doi.acm.org/10.1145/2499370.2462187>}, doi = {10.1145/2499370.2462187}, acmid = {2462187}, publisher = {ACM}, address = {New York, NY, USA}, keywords = {affine scheduling, autotuning, compiler optimization, loop transformations, program synthesis}, }

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author={Cummins, Chris and Petoumenos, Pavlos and Wang, Zheng and Leather, Hugh},

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title      = "Minimizing the cost of iterative compilation with active
learning",
keywords   = "Active Learning, Compilers, Iterative Compilation, Machine
Learning, Sequential Analysis;",
author     = "William Ogilvie and Pavlos Petoumenos and Zheng Wang and Hugh
Leather",
note      = "Date of Acceptance: 25/10/2016",
year      = "2016",
month     = "10",
booktitle = "The International Symposium on Code Generation and Optimization
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We describe the design of a convolutional neural network accelerator running on a Stratix V FPGA. The design runs at three times the throughput of previous FPGA CNN accelerator designs. We show that the throughput/watt is significantly higher than for a GPU, and project the performance when ported to an Arria 10 FPGA.

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{https://www.microsoft.com/en-us/research/publication/accelerating-deep-convolutional-neural-networks-using-specialized-hardware/}, address = {}, pages = {}, journal = {}, volume = {}, chapter =
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author    = {Audrunas Gruslys and
             R{\'}{e}mi Munos and
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title     = {Memory-Efficient Backpropagation Through Time},
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journal    = {CoRR},
volume    = {abs/1606.03401},
year      = {2016},
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{1994}, isbn = {1937-4151}, pages = {1-12}, url = {http://ieeexplore.ieee.org/document/273754/},
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