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journal     = {CoRR},
volume     = {abs/1410.0759},
year       = {2014},
url        = {http://arxiv.org/abs/1410.0759},
timestamp  = {Sun, 02 Nov 2014 11:25:59 +0100},
biburl     =
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title={Synthesizing benchmarks for predictive modeling},

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title = "Minimizing the cost of iterative compilation with active learning",

keywords = "Active Learning, Compilers, Iterative Compilation, Machine Learning, Sequential Analysis;",

author = "William Ogilvie and Pavlos Petoumenos and Zheng Wang and Hugh Leather",

note = "Date of Acceptance: 25/10/2016",

year = "2016",

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booktitle = "The International Symposium on Code Generation and Optimization (CGO) 2017",

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[download]

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We describe the design of a convolutional neural network accelerator running on a Stratix V FPGA. The design runs at three times the throughput of previous FPGA CNN accelerator designs. We show that the throughput/watt is significantly higher than for a GPU, and project the performance when ported to an Arria 10 FPGA.

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{10.1145/1344671.1344720}, acmid = {1344720}, publisher = {ACM}, address = {New York, NY,
USA}, keywords = {FPGA, FPGA accelerators, c-to-gates, high-performance computing, reconfigurable
computing}, } @inproceedings{Wong:2011:CFV:1950413.1950419, author = {Wong, Henry and Betz,
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fpga, soft processor}, }
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title     = {Memory-Efficient Backpropagation Through Time},
journal   = {CoRR},
volume    = {abs/1606.03401},
year      = {2016},
url       = {http://arxiv.org/abs/1606.03401},
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