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volume={35}, number={6}, pages={4-12}, keywords={computer architecture;digital
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title       = {cuDNN: Efficient Primitives for Deep Learning},
journal     = {CoRR},
volume     = {abs/1410.0759},
year       = {2014},
url        = {http://arxiv.org/abs/1410.0759},
timestamp  = {Sun, 02 Nov 2014 11:25:59 +0100},
biburl     =
{http://dblp.uni-trier.de/rec/bib/journals/corr/ChetlurWVCTCS14},
bibsource  = {dblp computer science bibliography, http://dblp.org}
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@article{Bao:2016:SDF:3012405.3011017, author = {Bao, Wenlei and Hong, Changwan and
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Sadayappan, P.}, title = {Static and Dynamic Frequency Scaling on Multicore CPUs}, journal = {ACM
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{26}, url = {http://doi.acm.org/10.1145/3011017}, doi = {10.1145/3011017}, acmid = {3011017},
publisher = {ACM}, address = {New York, NY, USA}, keywords = {Affine Programs, CPU Energy,
Static Analysis, Voltage and Frequency Scaling}, }
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Peng and Sadayappan, P. and Cong, Jason}, title = {Polyhedral-based Data Reuse Optimization for
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@article{Kong:2013:PTM:2499370.2462187, author = {Kong, Martin and Veras, Richard and Stock, Kevin and Franchetti, Franz and Pouchet, Louis-No\`{e}l and Sadayappan, P.}, title = {When Polyhedral Transformations Meet SIMD Code Generation}, journal = {SIGPLAN Not.}, issue_date = {June 2013}, volume = {48}, number = {6}, month = jun, year = {2013}, issn = {0362-1340}, pages = {127-138}, numpages = {12}, url = {<http://doi.acm.org/10.1145/2499370.2462187>}, doi = {10.1145/2499370.2462187}, acmid = {2462187}, publisher = {ACM}, address = {New York, NY, USA}, keywords = {affine scheduling, autotuning, compiler optimization, loop transformations, program synthesis}, }

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title={Synthesizing benchmarks for predictive modeling},

author={Cummins, Chris and Petoumenos, Pavlos and Wang, Zheng and Leather, Hugh},

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title = "Minimizing the cost of iterative compilation with active learning",

keywords = "Active Learning, Compilers, Iterative Compilation, Machine Learning, Sequential Analysis;",

author = "William Ogilvie and Pavlos Petoumenos and Zheng Wang and Hugh Leather",

note = "Date of Acceptance: 25/10/2016",

year = "2016",

month = "10",

booktitle = "The International Symposium on Code Generation and Optimization (CGO) 2017",

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We describe the design of a convolutional neural network accelerator running on a Stratix V FPGA. The design runs at three times the throughput of previous FPGA CNN accelerator designs. We show that the throughput/watt is significantly higher than for a GPU, and project the performance when ported to an Arria 10 FPGA.

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numpages = {1}, url = {http://doi.acm.org/10.1145/1344671.1344720}, doi =
{10.1145/1344671.1344720}, acmid = {1344720}, publisher = {ACM}, address = {New York, NY,
USA}, keywords = {FPGA, FPGA accelerators, c-to-gates, high-performance computing, reconfigurable
computing}, } @inproceedings{Wong:2011:CFV:1950413.1950419, author = {Wong, Henry and Betz,
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Microarchitecture}, booktitle = {Proceedings of the 19th ACM/SIGDA International Symposium on
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location = {Monterey, CA, USA}, pages = {5-14}, numpages = {10}, url =
{http://doi.acm.org/10.1145/1950413.1950419}, doi = {10.1145/1950413.1950419}, acmid =
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author    = {Audrunas Gruslys and
             R{\'}{e}mi Munos and
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title     = {Memory-Efficient Backpropagation Through Time},
journal   = {CoRR},
volume    = {abs/1606.03401},
year      = {2016},
url       = {http://arxiv.org/abs/1606.03401},
timestamp = {Fri, 01 Jul 2016 17:39:49 +0200},
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{1994}, isbn = {1937-4151}, pages = {1-12}, url = {http://ieeexplore.ieee.org/document/273754/},
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