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journal     = {CoRR},
volume     = {abs/1410.0759},
year       = {2014},
url        = {http://arxiv.org/abs/1410.0759},
timestamp  = {Sun, 02 Nov 2014 11:25:59 +0100},
biburl     =
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bibsource  = {dblp computer science bibliography, http://dblp.org}
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@article{Bao:2016:SDF:3012405.3011017, author = {Bao, Wenlei and Hong, Changwan and Chunduri, Sudheer and Krishnamoorthy, Sriram and Pouchet, Louis-Noël and Rastello, Fabrice and Sadayappan, P.}, title = {Static and Dynamic Frequency Scaling on Multicore CPUs}, journal = {ACM Trans. Archit. Code Optim.}, issue_date = {December 2016}, volume = {13}, number = {4}, month
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author={Cummins, Chris and Petoumenos, Pavlos and Wang, Zheng and Leather, Hugh},

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keywords   = "Active Learning, Compilers, Iterative Compilation, Machine
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author     = "William Ogilvie and Pavlos Petoumenos and Zheng Wang and Hugh
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note      = "Date of Acceptance: 25/10/2016",
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booktitle = "The International Symposium on Code Generation and Optimization
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= {Kalin Ovtcharov, Olatunji Ruwase, Joo-Young Kim, Jeremy Fowers, Karin Strauss, Eric Chung}, title
= {Accelerating Deep Convolutional Neural Networks Using Specialized Hardware}, booktitle = {},
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We describe the design of a convolutional neural network accelerator running on a Stratix V FPGA. The design runs at three times the throughput of previous FPGA CNN accelerator designs. We show that the throughput/watt is significantly higher than for a GPU, and project the performance when ported to an Arria 10 FPGA.

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{https://www.microsoft.com/en-us/research/publication/accelerating-deep-convolutional-neural-netwo
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