

@article{Bielecki:2016:TAN:3060371.3060383, author = {Bielecki, Włodzimierz and Pałkowski, Marek}, title = {Tiling Arbitrarily Nested Loops by Means of the Transitive}, journal = {Int. J. Appl. Math. Comput. Sci.}, issue_date = {12 2016}, volume = {26}, number = {4}, month = dec, year = {2016}, issn = {2083-8492}, pages = {919-939}, numpages = {21}, url = {<https://doi.org/10.1515/amcs-2016-0065>}, doi = {10.1515/amcs-2016-0065}, acmid = {3060383}, publisher = {Walter de Gruyter GmbH}, address = {Germany}, keywords = {iteration space slicing, polyhedral model, source-to-source compiler, tiling, transitive closure}, }

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@ARTICLE{7738524, author={Y. H. Chen and T. Krishna and J. S. Emer and V. Sze}, journal={IEEE Journal of Solid-State Circuits}, title={Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks}, year={2017}, volume={52}, number={1}, pages={127-138}, keywords={DRAM chips;data flow computing;energy conservation;feedforward neural nets;learning (artificial intelligence);neural net architecture;power aware computing;reconfigurable architectures;AI systems;AlexNet;CNN shapes;DRAM accesses;Eyeriss;MAC;RS dataflow reconfiguration;accelerator chip;convolutional layers;data movement energy cost;dataflow processing;deep convolutional neural networks;energy efficiency;energy-efficient reconfigurable accelerator;multiply and accumulation;off-chip DRAM;reconfiguring architecture;row stationary;spatial architecture;Clocks;Computer architecture;Hardware;Neural networks;Random access memory;Shape;Throughput;Convolutional neural networks (CNNs);dataflow processing;deep learning;energy-efficient accelerators;spatial architecture}, doi={10.1109/JSSC.2016.2616357}, ISSN={0018-9200}, month={Jan}, }

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Address = {New Delhi, India},
Author = {Rajopadhye, S. V. and Purushothaman, S. and Fujimoto, R. M.},
Booktitle = {Proceedings, Sixth Conference on Foundations of Software Technology and Theoretical Computer Science},
Key = {Rajopadhye86b},
Month = {December},
Pages = {488-503},
Publisher = {Springer Verlag, LNCS~241},
Title = {On Synthesizing Systolic Arrays from Recurrence Equations with Linear Dependencies},

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Year = {1986}}
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@article{quinton-jvsp89,
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  Author = {Quinton, P. and {Van Dongen}, V.},
  Journal = {Journal of {VLSI} Signal Processing},
  Number = 2,
  Pages = {95-113},
  Publisher = {Kluwer Academic Publishers, Boston},
  Title = {The Mapping of Linear Recurrence Equations on Regular
Arrays},
  Volume = 1,
  Year = 1989}
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references", journal= "International Journal of Parallel Programming", year= 1991, volume= 20,
number= 1, pages= "23-53", month= "Feb", annote= "This article explains how a simple imperative
language
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  program (consisting only of assignments, for loops with affine loop
  limits, and arrays with affine index expressions), can be statically
  analyzed to find the flow dependencies."
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title     = {Some Efficient Solutions to the Affine Scheduling Problem.
             {Part I}. One-dimensional Time},
journal   = {International Journal of Parallel Programming},
volume    = {21},
number    = {5},
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pages     = {313-347},
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title =       {Fuzzy Array Data Flow Analysis},
journal =     {Journal of Parallel and Distributed Computing},
year =        1997,
volume =      40,
number =      2,
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month =       {Feb}}
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title =       {The Polyhedral Model Is More Widely Applicable Than You Think},
booktitle =   {Proceedings of the International Conference on Compiler Construction ({ETAPS CC'10})},
year =        2010,
series =      {LNCS},
address =     {Paphos, Cyprus},
pages =       {283--303},
month =       Mar,
publisher =   {Springer-Verlag},
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@ARTICLE{7582549, author={U. Bondhugula and V. Bandishti and I. Pananilath}, journal={IEEE Transactions on Parallel and Distributed Systems}, title={Diamond Tiling: Tiling Techniques to Maximize Parallelism for Stencil Computations}, year={2016}, url={<http://ieeexplore.ieee.org/document/7582549/>}, volume={PP}, number={99}, pages={1-1}, keywords={Diamond;Face;Indexes;Optimization;Parallel processing;Shape;Silicon;Compilers;locality;loop tiling;parallelism;program transformation;stencils}, doi={10.1109/TPDS.2016.2615094}, ISSN={1045-9219}, month={},}

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              Cliff Woolley and
              Philippe Vandermersch and
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              John Tran and
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journal     = {CoRR},
volume     = {abs/1410.0759},
year       = {2014},
url        = {http://arxiv.org/abs/1410.0759},
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{http://dblp.uni-trier.de/rec/bib/journals/corr/ChetlurWVCTCS14},
bibsource  = {dblp computer science bibliography, http://dblp.org}
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@inproceedings{Pouchet:2013:PDR:2435264.2435273, author = {Pouchet, Louis-Noel and Zhang, Peng and Sadayappan, P. and Cong, Jason}, title = {Polyhedral-based Data Reuse Optimization for Configurable Computing}, booktitle = {Proceedings of the ACM/SIGDA International Symposium on Field Programmable Gate Arrays}, series = {FPGA '13}, year = {2013}, isbn = {978-1-4503-1887-7}, location = {Monterey, California, USA}, pages = {29-38}, numpages = {10}, url = {<http://doi.acm.org/10.1145/2435264.2435273>}, doi = {10.1145/2435264.2435273}, acmid = {2435273}, publisher = {ACM}, address = {New York, NY, USA}, keywords = {compilation, data reuse, high-level synthesis, program transformations}, }

@article{Kong:2013:PTM:2499370.2462187, author = {Kong, Martin and Veras, Richard and Stock, Kevin and Franchetti, Franz and Pouchet, Louis-Noel and Sadayappan, P.}, title = {When Polyhedral Transformations Meet SIMD Code Generation}, journal = {SIGPLAN Not.}, issue_date = {June 2013}, volume = {48}, number = {6}, month = jun, year = {2013}, issn = {0362-1340}, pages = {127-138}, numpages = {12}, url = {<http://doi.acm.org/10.1145/2499370.2462187>}, doi = {10.1145/2499370.2462187}, acmid = {2462187}, publisher = {ACM}, address = {New York, NY, USA}, keywords = {affine scheduling, autotuning, compiler optimization, loop transformations, program synthesis}, }

@article{cummins2017synthesizing,

title={Synthesizing benchmarks for predictive modeling},

author={Cummins, Chris and Petoumenos, Pavlos and Wang, Zheng and Leather, Hugh},

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title={Optimistic Loop Optimization},

author={Doerfert, Johannes and Grosser, Tobias and Hack, Sebastian},

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title      = "Minimizing the cost of iterative compilation with active
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keywords   = "Active Learning, Compilers, Iterative Compilation, Machine
Learning, Sequential Analysis;",
author     = "William Ogilvie and Pavlos Petoumenos and Zheng Wang and Hugh
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note      = "Date of Acceptance: 25/10/2016",
year      = "2016",
month     = "10",
booktitle = "The International Symposium on Code Generation and Optimization
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@inproceedings{Putnam:2014:RFA:2665671.2665678, author = {Putnam, Andrew and Caulfield,
Adrian M. and Chung, Eric S. and Chiou, Derek and Constantinides, Kypros and Demme, John and
Esmailzadeh, Hadi and Fowers, Jeremy and Gopal, Gopi Prashanth and Gray, Jan and Haselman,
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Sitaram and Larus, James and Peterson, Eric and Pope, Simon and Smith, Aaron and Thong, Jason and
Xiao, Phillip Yi and Burger, Doug}, title = {A Reconfigurable Fabric for Accelerating Large-scale
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{http://dl.acm.org/citation.cfm?id=2665671.2665678}, acmid = {2665678}, publisher = {IEEE
Press}, address = {Piscataway, NJ, USA}, }

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[download]

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@miscellaneous{accelerating-deep-convolutional-neural-networks-using-specialized-hardware, author
= {Kalin Ovtcharov, Olatunji Ruwase, Joo-Young Kim, Jeremy Fowers, Karin Strauss, Eric Chung}, title
= {Accelerating Deep Convolutional Neural Networks Using Specialized Hardware}, booktitle = {},
year = {2015}, month = {February}, abstract = {

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We describe the design of a convolutional neural network accelerator running on a Stratix V FPGA. The design runs at three times the throughput of previous FPGA CNN accelerator designs. We show that the throughput/watt is significantly higher than for a GPU, and project the performance when ported to an Arria 10 FPGA.

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{https://www.microsoft.com/en-us/research/publication/accelerating-deep-convolutional-neural-netwo
rks-using-specialized-hardware/}, address = {}, pages = {}, journal = {}, volume = {}, chapter =
{}, isbn = {}, }

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series = {ICS '01}, year = {2001}, isbn = {1-58113-410-X}, location = {Sorrento, Italy}, pages =
{65-77}, numpages = {13}, url = {http://doi.acm.org/10.1145/377792.377807}, doi =
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@article{DBLP:journals/corr/GruslysMDLG16,
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author = {Audrunas Gruslys and R{\'}mi Munos and Ivo Danihelka and Marc Lanctot and Alex Graves}, title = {Memory-Efficient Backpropagation Through Time}, journal = {CoRR}, volume = {abs/1606.03401}, year = {2016}, url = {http://arxiv.org/abs/1606.03401}, timestamp = {Fri, 01 Jul 2016 17:39:49 +0200}, biburl = {http://dblp.uni-trier.de/rec/bib/journals/corr/GruslysMDLG16}, bibsource = {dblp computer science bibliography, http://dblp.org}
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@inproceedings{FlowMap1994, author = {J. Cong and Ding, Yuzheng}, title = {FlowMap: an optimal technology mapping algorithm for delay optimization in lookup-table based FPGA designs}, booktitle = {IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems}, year = {1994}, isbn = {1937-4151}, pages = {1-12}, url = {http://ieeexplore.ieee.org/document/273754/}, doi = {10.1109/43.273754}, publisher = {IEEE} }
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