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linear recurrences into uniform recurrence equations. Both parts rely on results on integral convex polyhedra. Our results are illustrated on the Gauss elimination algorithm and on the Gauss-Jordan diagonalization algorithm.”, issn=“0922-5773”, doi=“10.1007/BF02477176”, url=“<https://doi.org/10.1007/BF02477176>” }

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 title = {Some Efficient Solutions to the Affine Scheduling Problem.
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 number = {5},
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 journal = {Journal of Parallel and Distributed Computing},
 year = 1997,

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number = 2,  
pages = {210-226},  
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series = {LNCS},  
address = {Paphos, Cyprus},  
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              Cliff Woolley and
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year      = {2014},
url       = {http://arxiv.org/abs/1410.0759},
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biburl    =
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We describe the design of a convolutional neural network accelerator running on a Stratix V FPGA. The design runs at three times the throughput of previous FPGA CNN accelerator designs. We show that the throughput/watt is significantly higher than for a GPU, and project the performance when ported to an Arria 10 FPGA.

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author      = {Audrunas Gruslys and  
              R{\'}mi Munos and  
              Ivo Danihelka and  
              Marc Lanctot and  
              Alex Graves},  
title       = {Memory-Efficient Backpropagation Through Time},  
journal     = {CoRR},  
volume     = {abs/1606.03401},  
year       = {2016},  
url        = {http://arxiv.org/abs/1606.03401},  
timestamp  = {Fri, 01 Jul 2016 17:39:49 +0200},  
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