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@ARTICLE{7738524, author={Y. H. Chen and T. Krishna and J. S. Emer and V. Sze}, journal={IEEE Journal of Solid-State Circuits}, title={Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks}, year={2017}, volume={52}, number={1}, pages={127-138}, keywords={DRAM chips;data flow computing;energy conservation;feedforward neural nets;learning (artificial intelligence);neural net architecture;power aware computing;reconfigurable architectures;AI systems;AlexNet;CNN shapes;DRAM accesses;Eyeriss;MAC;RS dataflow reconfiguration;accelerator chip;convolutional layers;data movement energy cost;dataflow processing;deep convolutional neural networks;energy efficiency;energy-efficient reconfigurable accelerator;multiply and accumulation;off-chip DRAM;reconfiguring architecture;row stationary;spatial architecture;Clocks;Computer architecture;Hardware;Neural networks;Random access memory;Shape;Throughput;Convolutional neural networks (CNNs);dataflow processing;deep learning;energy-efficient accelerators;spatial architecture}, url = {<http://ieeexplore.ieee.org/document/7738524/>}, doi={10.1109/JSSC.2016.2616357}, ISSN={0018-9200}, month={Jan},}

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linear recurrences into uniform recurrence equations. Both parts rely on results on integral convex polyhedra. Our results are illustrated on the Gauss elimination algorithm and on the Gauss-Jordan diagonalization algorithm.”, issn=“0922-5773”, doi=“10.1007/BF02477176”, url=“<https://doi.org/10.1007/BF02477176>” }

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program (consisting only of assignments, for loops with affine loop limits, and arrays with affine index expressions), can be statically analyzed to find the flow dependencies.”

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 title = {Some Efficient Solutions to the Affine Scheduling Problem.  
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 number = {5},  
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 journal = {Journal of Parallel and Distributed Computing},  
 year = 1997,

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booktitle = {Proceedings of the International Conference on Compiler Construction ({ETAPS CC'10})},  
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series = {LNCS},  
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pages = {283--303},  
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keywords={computer architecture;digital simulation;architectural layers;architectural
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journal   = {CoRR},
volume    = {abs/1410.0759},
year      = {2014},
url       = {http://arxiv.org/abs/1410.0759},
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We describe the design of a convolutional neural network accelerator running on a Stratix V FPGA. The design runs at three times the throughput of previous FPGA CNN accelerator designs. We show that the throughput/watt is significantly higher than for a GPU, and project the performance when ported to an Arria 10 FPGA.

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author      = {Audrunas Gruslys and  
              R{\'}mi Munos and  
              Ivo Danihelka and  
              Marc Lanctot and  
              Alex Graves},  
title       = {Memory-Efficient Backpropagation Through Time},  
journal     = {CoRR},  
volume     = {abs/1606.03401},  
year       = {2016},  
url        = {http://arxiv.org/abs/1606.03401},  
timestamp  = {Fri, 01 Jul 2016 17:39:49 +0200},  
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