# Schedule : Spring 2015

This is the tentative schedule of Mélange group for the Spring 2015 semester.

| WEEK | DATE | TOPIC | PRESENTER |
|---|---|---|---|
| 1 | 02/02/2015 | | |
| 2 | 02/09/2015 | Challenges for Future Computing Systems, by William J. Dally (NVIDIA) | Sanjay Rajopadhye |
| 3 | 02/16/2015 | No meeting | |
| 4 | 02/23/2015 | Going beyond the FPGA with Spacetime, by Steve Teig (Tabula) | Sanjay Rajopadhye |
| 5 | 03/02/2015 | Elevator talks with slides | Whole group |
| 6 | 03/09/2015 | • E. F. de O Sandes, A. C. M. A. de Melo, Smith-Waterman Alignment of Huge Sequences with GPU in Linear Space, Parallel Distributed Processing Symposium (IPDPS), 2011 IEEE International | Swetha Varadarajan |
| 7 | 03/16/2015 | Spring Break | |
| 8 | 03/23/2015 | No meeting | |
| 9 | 03/30/2015 | • R. Andonov, S. Rajopadhye, Knapsack on VLSI: From algorithm to optimal circuit, Parallel and Distributed Systems, IEEE Transactions on 1997 | Mugdha Puranik |
| 10 | 04/06/2015 | • Sanket Tavarageri, J Ramanujam, P Sadayappan, Adaptive parallel tiled code generation and accelerated auto-tuning, International Journal of High Performance Computing Applications 2013 | Waruna Ranasinghe |
| 11 | 04/13/2015 | • M. Shafique, S. Garg, T. Mitra, S. Parameswaran, J. Henkel, Dark silicon as a challenge for hardware/software co-design, Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2014 International Conference on | Revathy Rajasree |
| 12 | 04/20/2015 | • Venmugil Elango, Naser Sedaghati, Fabrice Rastello, Louis-Noël Pouchet, J. Ramanujam, Radu Teodorescu, P. Sadayappan, On Using the Roofline Model with Lower Bounds on Data Movement, ACM Trans. Archit. Code Optim. 2015 | Sanjay Rajopadhye |
| 13 | 04/27/2015 | Research Proposal | Guillaume Iooss |
| 15 | 05/04/2015 | TBD | TBD |

# Reading Pool

### Publications

**2015**

- Fabio Luporini, Ana Lucia Varbanescu, Florian Rathgeber, Gheorghe-Teodor Bercea, J. Ramanujam, David A. Ham, Paul H. J. Kelly, Cross-Loop Optimization of Arithmetic Intensity for Finite Element Local Assembly, 2015
- Venmugil Elango, Naser Sedaghati, Fabrice Rastello, Louis-Noël Pouchet, J. Ramanujam, Radu Teodorescu, P. Sadayappan, On Using the Roofline Model with Lower Bounds on Data Movement, 2015
- Martin Kong, Antoniu Pop, Louis-Noël Pouchet, R. Govindarajan, Albert Cohen, P. Sadayappan, Compiler/Runtime Framework for Dynamic Dataflow Parallelization of Tiled Programs, 2015
- Alessandro Cilardo, Luca Gallo, Improving Multibank Memory Access Parallelism with Lattice-Based Partitioning, 2015

**2014**

- R.L. Uy, Beyond multi-core: A survey of architectural innovations on microprocessor, 2014
- M. Shafique, S. Garg, T. Mitra, S. Parameswaran, J. Henkel, Dark silicon as a challenge for hardware/software co-design, 2014
- H.H.-W. Wang, L.Y.-Z. Lin, R.H.-M. Huang, C.H.-P. Wen, CASTA: CUDA-Accelerated Static Timing Analysis for VLSI Designs, 2014
- Rong Shi, Xiaoyi Lu, S. Potluri, K. Hamidouche, Jie Zhang, D.K. Panda, HAND: A Hybrid Approach to Accelerate Non-contiguous Data Movement Using MPI Datatypes on GPU Clusters, 2014
- J. Torrellas, Extreme-scale computer architecture: Energy efficiency from the ground up, 2014
- B.A. Hechtman, Shuai Che, D.R. Hower, Yingying Tian, B.M. Beckmann, M.D. Hill, S.K. Reinhardt, D.A. Wood, QuickRelease: A throughput-oriented approach to release consistency on GPUs, 2014
- M. Hayenga, V.R.K. Naresh, M.H. Lipasti, Revolver: Processor architecture for power efficient loop execution, 2014
- A. Ilic, F. Pratas, L. Sousa, Cache-aware Roofline model: Upgrading the loft, 2014
- Somnath Paul, Robert Karam, Swarup Bhunia, Ruchir Puri, Energy-efficient Hardware Acceleration Through Computing in the Memory, 2014

**2013**

- Sanket Tavarageri, J Ramanujam, P Sadayappan, Adaptive parallel tiled code generation and accelerated auto-tuning, 2013
- Tom Henretty, Richard Veras, Franz Franchetti, Louis-Noël Pouchet, J. Ramanujam, P. Sadayappan, A Stencil Compiler for Short-vector SIMD Architectures, 2013
- Fernando Machado Mendonca, Alba Cristina Magalhaes Alves de Melo, Biological Sequence Comparison on Hybrid Platforms with Dynamic Workload Adjustment, 2013

**2012**

- Jun Shirako, Kamal Sharma, Naznin Fauzia, Louis-Noël Pouchet, J. Ramanujam, P. Sadayappan, Vivek Sarkar, Analytical Bounds for Optimal Tile Size Selection, 2012

**2011**

- E. F. de O Sandes, A. C. M. A. de Melo, Smith-Waterman Alignment of Huge Sequences with GPU in Linear Space, 2011
- Louis-Noël Pouchet, Uday Bondhugula, Cédric Bastoul, Albert Cohen, J. Ramanujam, P. Sadayappan, Nicolas Vasilache, Loop Transformations: Convexity, Pruning and Optimization, 2011

**2000**

- R. Schreiber, S. Aditya, B.R. Rau, V. Kathail, S. Mahlke, S. Abraham, G. Snider, High-level synthesis of nonprogrammable hardware accelerators, 2000

**1997**

- R. Andonov, S. Rajopadhye, Knapsack on VLSI: From algorithm to optimal circuit, 1997