

Schedule : Fall 2015

This is the tentative schedule of Mélange group for the Fall 2015 semester.

WEEK	DATE	TOPIC	PRESENTER
1	08/25/2015	No meeting	
2	09/01/2015	• Mahesh Ravishankar, Roshan Dathathri, Venmugil Elango, Louis-Noël Pouchet, J. Ramanujam, Atanas Rountev, P. Sadayappan, Distributed Memory Code Generation for Mixed Irregular/Regular Computations , PPOPP 2015	Guillaume Iooss
3	09/08/2015	• Aravind Acharya, Uday Bondhugula, PLUTO+: Near-complete Modeling of Affine Transformations for Parallelism and Locality , PPOPP 2015	Swetha Varadarajan
4	09/15/2015	• Yuan Tang, Ronghui You, Haibin Kan, Jesmin Jahan Tithi, Pramod Ganapathi, Rezaul A. Chowdhury, Cache-oblivious Wavefront: Improving Parallelism of Recursive Dynamic Programming Algorithms Without Losing Cache-efficiency , PPOPP 2015	Waruna Ranasinghe
5	09/22/2015	• Kevin Stock, Martin Kong, Tobias Grosser, Louis-Noël Pouchet, Fabrice Rastello, J. Ramanujam, P. Sadayappan, A Framework for Enhancing Data Reuse via Associative Reordering , PLDI '14	Nirmal Prajapati
6	09/29/2015	• Jason Cong, Peng Li, Bingjun Xiao, Peng Zhang, An Optimal Microarchitecture for Stencil Computation Acceleration Based on Non-Uniform Partitioning of Data Reuse Buffers , DAC '14	Rajbharath Chandramohan
7	10/06/2015	Practice Talk	Mugdha Puranik
8	10/13/2015	• N. Agarwal, D. Nellans, M. O'Connor, S.W. Keckler, T.F. Wenisch, Unlocking bandwidth for GPUs in CC-NUMA systems , High Performance Computer Architecture (HPCA), 2015 IEEE 21st International Symposium	Venkatesh Babu
9	10/20/2015	• Uday Bondhugula, Vinayaka Bandishti, Albert Cohen, Guillaín Potron, Nicolas Vasilache, Tiling and Optimizing Time-iterated Computations on Periodic Domains , PACT '14	Yun Zou
10	10/27/2015	No meeting	
11	11/03/2015	• M. Hayenga, V.R.K. Naresh, M.H. Lipasti, Revolver: Processor architecture for power efficient loop execution , High Performance Computer Architecture (HPCA), 2014 IEEE 20th International Symposium	Prerana Ghalsasi
12	11/10/2015	• Austin R. Benson, Grey Ballard, A Framework for Practical Parallel Fast Matrix Multiplication , PPOPP 2015	Revathy Rajasree

WEEK	DATE	TOPIC	PRESENTER
13	11/17/2015	• Alessandro Cilardo, Luca Gallo, Improving Multibank Memory Access Parallelism with Lattice-Based Partitioning , ACM Trans. Archit. Code Optim. 2015	Swetha Varadarajan
14	11/24/2015	Fall Break	
15	12/01/2015	Background - • Somashekaracharya G Bhaskaracharya, Uday Bondhugula, Albert Cohen, Automatic Intra-Array Storage Optimization , IISc-CSA-TR-2014-3, Nov 2014 and submitted to ACM TOPLAS, Feb 2015	Sanjay Rajopadhye
16	12/08/2015	• Somashekaracharya G Bhaskaracharya, Uday Bondhugula, Albert Cohen, Automatic Intra-Array Storage Optimization , IISc-CSA-TR-2014-3, Nov 2014 and submitted to ACM TOPLAS, Feb 2015	Sanjay Rajopadhye

Reading Pool

Publications

2015

- J.J. Tithi, P. Ganapathi, A. Talati, S. Aggarwal, R. Chowdhury, High-Performance Energy-Efficient Recursive Dynamic Programming with Matrix-Multiplication-Like Flexible Kernels, 2015
- N. Agarwal, D. Nellans, M. O'Connor, S.W. Keckler, T.F. Wenisch, Unlocking bandwidth for GPUs in CC-NUMA systems, 2015
- Alessandro Cilardo, Luca Gallo, Improving Multibank Memory Access Parallelism with Lattice-Based

Partitioning, 2015

- Aravind Acharya, Uday Bondhugula, PLUTO+: Near-complete Modeling of Affine Transformations for

Parallelism and Locality, 2015

- Yuan Tang, Ronghui You, Haibin Kan, Jesmin Jahan Tithi, Pramod Ganapathi, Rezaul A. Chowdhury, Cache-oblivious Wavefront: Improving Parallelism of Recursive Dynamic Programming Algorithms Without Losing Cache-efficiency, 2015
- Mohamed Wahib, Naoya Maruyama, Automated GPU Kernel Transformations in Large-Scale Production Stencil Applications, 2015
- Austin R. Benson, Grey Ballard, A Framework for Practical Parallel Fast Matrix Multiplication, 2015
- Mahesh Ravishankar, Roshan Dathathri, Venmugil Elango, Louis-Noël Pouchet, J. Ramanujam,

Atanas Rountev, P. Sadayappan, Distributed Memory Code Generation for Mixed Irregular/Regular Computations, 2015

- Somashekaracharya G Bhaskaracharya, Uday Bondhugula, Albert Cohen, Automatic Intra-Array Storage Optimization, 2015

2014

- K. Sano, Y. Hatsuda, S. Yamamoto, Multi-FPGA Accelerator for Scalable Stencil Computation with Constant Memory Bandwidth, 2014
- M. Hayenga, V.R.K. Naresh, M.H. Lipasti, Revolver: Processor architecture for power efficient loop execution, 2014
- Uday Bondhugula, Vinayaka Bandishti, Albert Cohen, Guillain Potron, Nicolas Vasilache, Tiling and Optimizing Time-iterated Computations on Periodic Domains, 2014
- Cheng-Chieh Huang, Vijay Nagarajan, ATCache: Reducing DRAM Cache Latency via a Small SRAM Tag Cache, 2014
- Ehsan Fatehi, Paul Gratz, ILP and TLP in Shared Memory Applications: A Limit Study, 2014
- Robert D. Cameron, Thomas C. Shermer, Arrvindh Shriraman, Kenneth S. Herdy, Dan Lin, Benjamin R. Hull, Meng Lin, Bitwise Data Parallelism in Regular Expression Matching, 2014
- Jason Ansel, Shoaib Kamil, Kalyan Veeramachaneni, Jonathan Ragan-Kelley, Jeffrey Bosboom, Una-May O'Reilly, Saman Amarasinghe, OpenTuner: An Extensible Framework for Program Autotuning, 2014
- Nitin Sukhija, Brandon Malone, Srishti Srivastava, Ioana Banicescu, Florina M. Ciorba, Portfolio-Based Selection of Robust Dynamic Loop Scheduling Algorithms Using Machine Learning, 2014
- Ananta Tiwari, Anthony Gamst, Michael A. Laurenzano, Martin Schulz, Laura Carrington, Modeling the Impact of Reduced Memory Bandwidth on HPC Applications, 2014
- Jianbin Fang, Henk Sips, LiLun Zhang, Chuanfu Xu, Yonggang Che, Ana Lucia Varbanescu, Test-driving Intel Xeon Phi, 2014
- Jason Cong, Peng Li, Bingjun Xiao, Peng Zhang, An Optimal Microarchitecture for Stencil Computation Acceleration Based on Non-Uniform Partitioning of Data Reuse Buffers, 2014
- Kevin Stock, Martin Kong, Tobias Grosser, Louis-Noël Pouchet, Fabrice Rastello, J. Ramanujam, P. Sadayappan, A Framework for Enhancing Data Reuse via Associative Reordering, 2014

2013

- Alexandre S. Nery, Lech Jozwiak, Menno Lindwer, Mauro Cocco, Nadia Nedjah, Felipe M. G. Franca, Hardware Reuse in Modern Application-specific Processors and

Accelerators, 2013

- Mitesh R. Meswani, Laura Carrington, Didem Unat, Allan Snaveley, Scott Baden, Stephen Poole, Modeling and Predicting Performance of High Performance Computing

Applications on Hardware Accelerators, 2013

- Dave G. Wonnacott, Michelle Mills Strout, On the Scalability of Loop Tiling Techniques, 2013

2012

- Changyou Zhang, Kun Huang, Xiang Cui, Yifeng Chen, Power-aware Programming with GPU Accelerators, 2012
- Vinayaka Bandishti, Irshad Pananilath, Uday Bondhugula, Tiling Stencil Computations to Maximize Parallelism, 2012

2009

- M. Shafiq, M. Pericas, R. de la Cruz, M. Araya-Polo, N. Navarro, E. Ayguade, Exploiting memory customization in FPGA for 3D stencil computations, 2009

2006

- Kevin Fan, Manjunath Kudlur, Hyunchul Park, Scott Mahlke, Increasing Hardware Efficiency with Multifunction Loop

Accelerators, 2006

1991

- William Pugh, The Omega Test: A Fast and Practical Integer Programming Algorithm

for Dependence Analysis, 1991

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