Schedule : Spring 2017

This is the tentative schedule of Mélange group for the Spring 2017 semester.

Mélange

Purpose: Recent research paper study and discussion from the Reading pool
Meet time & Place : Wednesdays 10:00 AM - 11:00 AM @ CSB 305

WEEK	DATE	TOPIC	PRESENTER
0	08/23/2017	No Meeting	
2	01/25/2017	• Wenlei Bao, Changwan Hong, Sudheer Chunduri, Sriram Krishnamoorthy, Louis-Noel Pouchet, Fabrice Rastello, P. Sadayappan, Static and Dynamic Frequency Scaling on Multicore CPUs, ACM Trans. Archit. Code Optim. 2016	Loius-Noel Pouchet
3	02/01/2017	Practice Talk	Nirmal Prajapati
4	02/08/2017	• Chris Cummins, Pavlos Petoumenos, Zheng Wang, Hugh Leather, Synthesizing benchmarks for predictive modeling	Steve Kommrusch
5	02/15/2017	• Vinayaka Bandishti, Irshad Pananilath, Uday Bondhugula, Tiling Stencil Computations to Maximize Parallelism, SC '12	Laurette Hamlin
6	02/22/2017	CSU Faculty Candidate Seminar by Dr. David Crandall	-
7	03/01/2017	• T. Nowatzki, J. Menon, C. H. Ho, K. Sankaralingam, Architectural Simulators Considered Harmful, IEEE Micro 2015	Daniel Ball
8	03/08/2017	CSU Faculty Candidate Seminar	-
9	03/15/2017	TBD	Spring Break
10	03/22/2017	• J. D. Garvey, T. S. Abdelrahman, Automatic Performance Tuning of Stencil Computations on GPUs, 2015 44th International Conference on Parallel Processing	Prerana Ghalsasi
11	03/29/2017	• Daniel J. Milroy, Allison H. Baker, Dorit M. Hammerling, John M. Dennis, Sheri A. Mickelson, Elizabeth R. Jessup, Towards Characterizing the Variability of Statistically Consistent Community Earth System Model Simulations, Procedia Computer Science 2016	Sheri Mickelson
12	04/05/2017	Discussion- Codesign Paper results	Nirmal Prajapati
13	04/12/2017	• A. Pedram, A. Gerstlauer, R. A. v. d. Geijn, A high-performance, low-power linear algebra core, ASAP 2011 - 22nd IEEE International Conference on Application-specific Systems, Architectures and Processors	Saahil Kitture

WEEK	DATE	TOPIC	PRESENTER
14	04/19/2017	• J. Ramanujam Sanket Tavarageri, P. Sadayappan, Parametric Tiling of Affine Loop Nests	Louis-Noel Pouchet
15	04/26/2017	TBD	Steven Quinito
16	05/03/2017	TBD	Waruna Ranasinghe
17	05/10/2017	TBD	Tarequl Sifat
18	05/17/2017	TBD	Swetha Varadrajan

Reading Pool

Publications

2017

- Johannes Doerfert, Tobias Grosser, Sebastian Hack, Optimistic Loop Optimization, 2017
- Chris Cummins, Pavlos Petoumenos, Zheng Wang, Hugh Leather, Synthesizing benchmarks for predictive modeling, 2017

2016

- Wenlei Bao, Changwan Hong, Sudheer Chunduri, Sriram Krishnamoorthy, Louis-Noel Pouchet, Fabrice Rastello, P. Sadayappan, Static and Dynamic Frequency Scaling on Multicore CPUs, 2016
- William Ogilvie, Pavlos Petoumenos, Zheng Wang, Hugh Leather, Minimizing the cost of iterative compilation with active learning, 2016
- Daniel J. Milroy, Allison H. Baker, Dorit M. Hammerling, John M. Dennis, Sheri A. Mickelson, Elizabeth R. Jessup, Towards Characterizing the Variability of Statistically Consistent Community Earth System Model Simulations, 2016
- Audrunas Gruslys, R{ '{e}}mi Munos, Ivo Danihelka, Marc Lanctot, Alex Graves, Memory-Efficient Backpropagation Through Time, 2016
- U. Bondhugula, V. Bandishti, I. Pananilath, Diamond Tiling: Tiling Techniques to Maximize Parallelism for Stencil Computations, 2016

2015

- T. Nowatzki, J. Menon, C. H. Ho, K. Sankaralingam, Architectural Simulators Considered Harmful, 2015
- J. D. Garvey, T. S. Abdelrahman, Automatic Performance Tuning of Stencil Computations on GPUs, 2015
- Eric Chung Kalin Ovtcharov, Accelerating Deep Convolutional Neural Networks Using Specialized

Hardware, 2015

- Protonu Basu, Mary Hall, Samuel Williams, Brian Van Straalen, Leonid Oliker, Phillip Colella, Compiler-Directed Transformation for Higher-Order Stencils, 2015

2014

- Andrew Putnam, Adrian M. Caulfield, Eric S. Chung, Derek Chiou, Kypros Constantinides, John Demme, Hadi Esmaeilzadeh, Jeremy Fowers, Gopi Prashanth Gopal, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, Joo-Young Kim, Sitaram Lanka, James Larus, Eric Peterson, Simon Pope, Aaron Smith, Jason Thong, Phillip Yi Xiao, Doug Burger, A Reconfigurable Fabric for Accelerating Large-scale Datacenter Services, 2014
- Sharan Chetlur, Cliff Woolley, Philippe Vandermersch, Jonathan Cohen, John Tran, Bryan Catanzaro, Evan Shelhamer, cuDNN: Efficient Primitives for Deep Learning, 2014

2013

- Martin Kong, Richard Veras, Kevin Stock, Franz Franchetti, Louis-No “{e}l Pouchet, P. Sadayappan, When Polyhedral Transformations Meet SIMD Code Generation, 2013
- Louis-Noel Pouchet, Peng Zhang, P. Sadayappan, Jason Cong, Polyhedral-based Data Reuse Optimization for Configurable Computing, 2013

2012

- Vinayaka Bandishti, Irshad Pananilath, Uday Bondhugula, Tiling Stencil Computations to Maximize Parallelism, 2012

2011

- A. Pedram, A. Gerstlauer, R. A. v. d. Geijn, A high-performance, low-power linear algebra core, 2011
- Henry Wong, Vaughn Betz, Jonathan Rose, Comparing FPGA vs. Custom Cmos and the Impact on Processor Microarchitecture, 2011

2010

- J. Ramanujam Sanket Tavarageri, P. Sadayappan, Parametric Tiling of Affine Loop Nests, 2010

2008

- Andrew R. Putnam, Dave Bennett, Eric Dellinger, Jeff Mason, Prasanna Sundararajan, CHiMPS: A High-level Compilation Flow for Hybrid CPU-FPGA Architectures, 2008

2001

- Steven J. Deitz, Bradford L. Chamberlain, Lawrence Snyder, Eliminating Redundancies in Sum-of-product Array Computations, 2001

1994

- J. Cong, Yuzheng Ding, FlowMap: an optimal technology mapping algorithm for delay optimization in lookup-table based FPGA designs, 1994