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Fault Modeling and Design for Testability of Emitter Coupled Logic (ECL) *

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Abstract

Bipolar Emitter Coupled Logic (ECL) devices can now be fabricated at higher densities and with lower power consumption. Behaviour of simple and complex ECL gates are examined in the presence of physical faults. The effectiveness of the classical stuck-at model in representing physical failures in ECL gates is examined. It is shown that the conventional stuck-at fault model cannot represent a majority of circuit level faults. A new augmented stuck-at fault model is presented which provides a significantly higher coverage of physical failures. A design for testability approach is presented for on-line detection of certain error conditions occurring in gates with true and complementary outputs which is a normal implementation for ECL devices.

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1 Introduction

Emitter Coupled Logic (ECL) using bipolar technology is a non-saturated form of digital logic which eliminates transistor storage time as a speed limiting characteristic, permitting very high speeds of operation [1]. Conventional bipolar ECL technology represents the state of the art in silicon speed, providing system propagation delays of the order of 300 to 500 pico seconds but the price paid for such speeds is very high power dissipation (1.5 mW or more per gate - way too much for VLSI densities) [2]. Transistor size and circuit density are two factors causing high power dissipation. Some recent developments in technology such as BIT1 [2] developed by Bipolar Integrated Technology have made it possible to create smaller bipolar transistors and ECL devices are being fabricated at higher densities and much lower power. A BIT1 transistor takes about 1/20 th the area of present day conventional ECL devices and the speed is comparable to the fastest ECL transistors which is achieved at 1/10th the power [2].

With the attainment of low power, high speed, as well as high density, ECL technology is expected to be used widely in various high performance digital circuits. For example, Sparc architecture developed by Sun microsystem, is being implemented using BIT's new bipolar process [3]. The B5000 ECL Sparc series of components represents a new approach to constructing high performance computer systems at a relatively low cost, using which they are able to design small ECL systems that perform at a level equal to large mainframe computers and approach that of present day supercomputers [3]. The integrated ECL microprocessor chip contains 122,000 transistors. Even more highly integrated bipolar and bipolar/MOS chips are expected in future, further narrowing the gap between low cost workstations and high performance servers [3].

Transistor level shorts and opens model many of the physical failures and defects in IGs [4]. A study performed by Gailiay [5] on 4-bit MOS microprocessor chips revealed that a great majority of faults were shorts and opens at the transistor. Defects and failures in present day integrated circuits can be abstracted to shorts and opens in the interconnects and degradation of devices [6]. Therefore, fault models at the transistor level, can characterize failures quite accurately [5, 7, 8, 9, 10, 11, 12]. For MOS devices it has been shown that gate level models may not correctly represent some major failure modes [13 , 14, 15]. Analysis of faults in simple logic circuits suggest that transistor level testing provides a higher coverage of faults compared to that at gate level [16]. It is necessary to study the effects of failures at the transistor level and develop accurate fault models at this level [4]. The major fault models at transistor level are stuck-at faults, stuck-shorts

and opens of transistor and interconnects, and bridging faults [17].

In this paper, we first examine an ECL OR/NOR gate for various physical failures and its effects. SPICE simulations are used to study and compare analytical results to ensure that there are no inconsistencies or inaccurate assumptions. Delay faults due to various physical failures are not considered in this study. Various physical failures are compared with the classical stuck-at fault model and fault coverage is obtained. We propose an augmented stuck-at fault model which provides a higher coverage of physical failures. We extend this philosophy to 2-level complex ECL gates to obtain a generalized fault model. Morandi et. al. [18] have proposed an ECL logic model obtained using the dictionary for translating each circuit element into a gate level description, which results in a complicated logic model even for a simple ECL OR/NOR circuit description. The proposed augmented stuck-at fault model is much simpler than the logic model proposed in [18]. A testable design approach is presented to detect certain error conditions, termed IIKE errors, exhibited by gates having true and complementary outputs. Certain defects during manufacturing process lead to a short in the integrated circuit causing excessive current to be drawn by the device. One such fault exhibits delay fault, and detection such delay faults in a device is much more difficult. We present a built-in current sensing technique for detecting such faults.

This paper is organized as follows. In section 2, a brief description of Emitter Coupled Logic and ECL OR/NOR gate operation is given. Sections 3 and 4 deal with the analysis of physical defects, application of classical stuck-at fault model and proposed augmented stuck-at fault model of one-level and two-level ECL gates respectively. In Section 5, power supply current monitoring technique to detect certain manufacturing defects in ECL devices is presented. A testable design approach is presented in Section 6 and finally conclusions are given in Section 7.

2 Emitter Coupled Logic

Schottky TTL produces speed improvement by prevention of saturation but ECL uses differential amplifier configuration to control current levels so as to avoid saturation. Control of emitter current or collector current is achieved using the differential amplifier circuit shown in Figure 1. Transistors Q_1 and Q_2 are arranged in a differential amplifier configuration. The transistor Q_1 conducts in its active region as long as input V_{in} is less than V_1 which is grounded as shown in Figure 1. When V_{in} starts exceeding V_1, the current I_E through R_3 divides between transistors Q_1 and Q_2. As V_{in} starts exceeding V_1 even by a small amount, Q_1 turns OFF and Q_2 turns ON

Figure 1: A Differential Amplifier.

fully remaining in the active region. The collector outputs of both the transistors are always in opposite states. The collectors of Q_1 and Q_2 provide complementary output signals. This amplifier with the addition of emitter follower output stages forms the basis of ECL basic OR/NOR gate [19]. Emitter Coupled refers to the manner in which the emitters of the differential amplifier are connected within the integrated circuit [19]. The differential amplifier provides high input impedances and voltage gain within the circuit. Emitter follower outputs restore the logic levels and provide low output impedance for good line driving and high fan-out capability [1].

Figure 2 shows the block diagram of a fundamental ECL gate which consists of a current steering differential amplifier connected by inputs, a temperature and voltage compensated bias network for providing stable voltage bias to the differential amplifier and emitter follower outputs. Figure 3 shows the basic gate circuit diagram, of the Motorola MECL 10K family [1] which is being used as the basic building block in most implementations of current day ECL logic designs.

The operation of a basic ECL OR/NOR gate can be explained by referring to Figure 3. Transistors Q_1, Q_2 along with Q_3 form a differential amplifier with base voltage of Q_3 (VB_3) derived from an internal reference circuit. The transistor stage Q_4 is a temperature and voltage compensation network to provide stable reference (V_{BB}) at about the center of the output voltage swing. The functioning of the ECL OR/NOR gate can be summarized as follows: The transistor Q_3 will conduct only when the input transistors (Q_1) and (Q_2) are held OFF with low input voltages as (V_{IL}). As soon as any one of the transistors is turned ON (i.e. an input transition to V_{IH}), Q_3

Figure 3: Circuit diagram of a 2-input ECL OR/NOR gate.

turns OFF. Turning OFF of Q_3 causes output of Q_5 (OR output) to go to V_{OH} and that of Q_6 (NOR output) to go to V_{OL}. Similarly, when the input signals revert to low state, Q_1 and Q_2 are turned OFF again and Q_3 gets turned ON. The collector voltages resulting from the switching action of Q_1, Q_2 and Q_3 are transferred through the emitter followers to the output terminals. Hence, the circuit provides logic OR and NOR functions in positive logic, or AND and NAND in the negative logic. No inverters are needed in ECL since every gate provides a direct as well as a complemented output.

The input transistors have their bases held to the V_{EE} line by the pull-down resistors (R_1 and R_2) which provide a leakage current path. Unused input terminals can be left floating without risk of noise coupling to the differential amplifier inputs. The 50 Kohm input resistances maintain logic '0' at inputs with inputs disconnected. The emitter follower output provides sufficient drive capability and also changes the output voltage levels so that the input high and low voltages are compatible. The output of emitter followers are left open without internal load resistances, which allows the connection of matching transmission line and matching impedance/loads at the receive end according to the user requirement which increases speed and reduces power consumption. When using the faster type ECL gate with no output pull-down resistance, there is a choice of a load resistance between using 50 ohm to -2 V or using 510 ohm to the V_{EE} line. A 50 ohm resistor connected to -2 V is commonly used when transmission lines are used for driving. In practice, V_{CC1} and V_{CC2} are connected to ground and V_{EE} is connected to -5.2 V.

The reference voltage V_{BB} which tracks V_{CC} is approximately -1.3 V. The reason for using separate V_{CC} connections ($V_{CC1,2}$ being connected to ground) is to minimize the effects of crosstalk interference from fast transients. The output logic levels are between -1.63V and -1.85V for V_{OL} and -0.810V and -0.980 for V_{OH}. Transistor Q_4 along with the diode and resistor network forms the temperature and voltage compensated bias network. Transistors Q_5 and Q_6 constitute the emitter follower outputs. Resistors R_9 and R_{10} are connected externally and are not provided internally by the ECL OR/NOR gate. The logic voltage levels for MECL 10K gates are shown in Figure 4.

Just like complex gates in nMOS and CMOS, multilevel implementations are possible in ECL. One of the techniques is called series gating in which transistor pairs are 'stacked' one above the other in 'tiers' so that current can be steered through different paths. This technique is illustrated in Figure 5 where there are two tiers of transistor pairs implementing the function $(A+B).(C+D)$ and its complement $\overline{(A+B).(C+D)}$. The penalty for the additional functionality is an increase

Figure 4: Output and Input ECL voltage levels.

in the propagation delay; however, this generally is less than in the case where the function is decomposed into two or more gates [3]. Series gating techniques are used, for example, in construction of shift registers that make up the diagnostic chain in the Integer Unit (IU) and floating-point controller (FPC) [3].

3 Fault Modeling of the ECL OR/NOR Gate

3.1 Analysis of Physical Defects

In this section, we evaluate the response of the basic ECL OR/NOR gate for various faults. Before performing defect analysis and fault modeling, basic circuit operation, bias conditions, interface constraints have been verified. A list of possible hard failures (opens, shorts etc.) which affect the circuit functionality is obtained. Possible hard failures considered here include all possible opens and shorts of transistors, diodes and resistors, transistor junction opens and shorts.

ECL OR/NOR gate circuit outputs are obtained after performing analysis for all input vectors by simulating one failure at a time for all the possible hard failures (opens, shorts etc.) of all the devices (transistors, diodes and resistors). The ECL OR/NOR gate outputs obtained analytically have been compared with the SPICE [20] simulation outputs to ensure that there are no inconsistencies or inaccurate assumptions.

Although the standard specified V_{IL} is between -1.85 V and -1.475 V, SPICE [20] simulations indicate that an input between -2.00 V and -1.475 V is also recognized by a logic gate as valid logic '0'. Similarly, though the specified V_{IH} is between -1.105 V and -0.810 V, an input between -1.105

Figure 5: Two-level series gating implementation.

Table 1: List of Fault groups vs Physical failures.

ff: Fault-free, $R1/R2$ Open.
$f1$: $Q1$ Emitter/Base Open.
$f2$: $Q1$ Collector Open.
$f3$: $Q2$ Emitter/Base Open.
$f4$: $Q2$ Collector Open.
$f5$: $Q3$ Emitter/Base Open, $Q4$ Emitter/Base/ Collector Open, $R6$ Open, $Q1/Q2$ Short.
$f6$: $Q3$ Collector Open, $Q5$ Short, $Q6$ Base to Collector Short.
$f7$: $Q5$ Emitter/Base/Collector Open, $R4$ Open, $Q5$ Base to Emitter Short.
$f8$: $Q6$ Emitter/Base/Collector Open, $R3$ Open, $Q1/Q2$ Base to Collector Short $Q6$ Base to Emitter Short.
$f9$: $R5$ Open, $Q3$ Base to Emitter Short.
$f10$: $R7$ Open, $Q4$ Base to Emitter Short.
$f11$: $R8/D1/D2$ Open, $Q3/Q4$ Short, $Q4$ Base to Collector Short.
$f12$: $R9$ Open.
$f13$: $R10$ Open.
$f14$: $Q6$ Short, $Q6$ Base to Collector Short.
$f15$: $Q1$ Base to Emitter Short.
$f16$: $Q2$ Base to Emitter Short.
$f17$: $Q3$ Base to Collector Short.

Table 2: Circuit behaviour under physical failures (ff=Fault-free, $f1$-$f17$=Defective).

ECL OR/NOR Gate Stuck Open/Short Analysis									
Input	ff	$f1$	$f2$	$f3$	$f4$	$f5$	$f6$	$f7$	$f8$
A B	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y
0 0	0 1	0 1	0 1	0 1	0 1	1 0	1 1	0 1	0 0
0 1	1 0	1 0	1 0	0 1	1 1	1 0	1 0	0 0	1 0
1 0	1 0	0 1	1 1	1 0	1 0	1 0	1 0	0 0	1 0
1 1	1 0	1 0	1 0	1 0	1 0	1 0	1 0	0 0	1 0

Input	$f9$	$f10$	$f11$	$f12$	$f13$	$f14$	$f15$	$f16$	$f17$
A B	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y
0 0	1 1	0 1	0 1	U 1	0 1	0 1	1 1	1 1	0 1
0 1	1 1	1 0	0 1	1 0	1 U	1 1	1 0	1 1	0 U
1 0	1 1	1 0	0 1	1 0	1 U	1 1	1 1	1 0	0 U
1 1	1 1	1 0	0 1	1 0	1 U	1 1	1 1	1 1	0 U

X=OR Output, Y=NOR Output, U=Undefined.

V and 0.00 V is also recognized as logic '1'. These values could occur in faulty logic gates. The intermediate voltage level between -1.475 V and -1.105 V is termed 'Undefined' (U) logic level.

Table 1 lists the various fault groups and the physical failures considered. This includes all opens and shorts of transistors, diodes and resistors, transistor junction opens and shorts. The output of the circuit behavior obtained under various defects are tabulated by combining and grouping the various faults as shown in Table 2. It can be seen that only the fault groups $f12$, $f13$ and $f17$ cause an undefined logic level. Fault groups $f12$ (True output) $f13$ (Complementary output) and $f17$ (Complementary output) are undetectable at logic level as there are no input patterns for which the faulty and fault-free gate provide opposite logic values at any of the outputs.

An interesting observation which needs mentioning is that of the physical failure $R1/R2$ short. The purpose of the input resistances are to maintain the inputs at logic '0' with inputs disconnected. If an ECL gate with $R1$ or $R2$ short is driven by another ECL gate with output equal to logic '1', then the -5.2V appearing at the input due to the short of input resistance will dominate causing the input to appear as logic '0'. It has been verified with SPICE [20] simulation that the input then effectively appears stuck at 0. Diodes $D1/D2$ serve the purpose of temperature compensation and shorting only causes degradation of temperature compensation performance. Some of the fault groups represent effects of several equivalent faults.

Figure 6: Classical stuck-at fault model.

Table 3: ECL OR/NOR Gate outputs for Classical Stuck-at fault model.

ECL OR/NOR Gate Classical Stuck-at fault model									
Input	ff	A_1	B_1	A_0	B_0	X_1	Y_1	X_0	Y_0
A B	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y
0 0	0 1	1 0	1 0	0 1	0 1	1 1	0 1	0 1	0 0
0 1	1 0	1 0	1 0	1 0	0 1	1 0	1 1	0 0	1 0
1 0	1 0	1 0	1 0	0 1	1 0	1 0	1 1	0 0	1 0
1 1	1 0	1 0	1 0	1 0	1 0	1 0	1 1	0 0	1 0

X=OR Output, Y=NOR Output, ff=Fault-free

3.2 Effectiveness of Classical Stuck-at fault model

In order to model the physical failures, the classical stuck-at fault model is applied to the ECL OR/NOR gate as shown in Figure 6. Results shown in Table 3 were obtained by exercising the model with all possible input combinations for fault-free as well as faulty conditions by introducing one stuck-fault at a time. In Table 3, the subscripts 0 and 1 are used to represent stuck at 0 and 1 respectively. For example, X_0 indicates stuck-at-0 on X and X_1 indicates stuck-at-1 on X. The defective circuit behavior (Table 2) now can be compared with the classical stuck-at fault model output (Table 3) to obtain the effectiveness of the stuck at model in representing various component failures.

Correlation between OR/NOR gate classical stuck-at fault model output and physical failures is shown in columns 1-3 of Table 4, where it can be seen that all the classical stuck-at faults model some physical failures. In Table 3, A_1/B_1 indicates A stuck at 1 or B stuck at 1. The physical failures as modeled by fault-groups $f1$, $f3$, $f5$, $f6$, $f7$, $f8$ and $f14$ are modeled accurately using the classical stuck-at fault model. The faults $f12$, $f13$ and $f17$ cause one of the output to become indeterminate, which cannot be represented by a logical fault model. From the rest, the classical

Figure 7: Proposed augmented stuck-at fault model.

stuck-at fault model leaves 7 fault groups uncovered, corresponding to 14 physical failures. In the next section, we present an augmented stuck-at fault model that provides a higher coverage of physical failures compared to the classical stuck-at fault model.

3.3 An Augmented Stuck-at fault model

The classical input/output stuck-at fault model is not effective for modeling ECL gates. Figure 7 shows the proposed augmented stuck-at fault model which improves the fault coverage. Here, the device is modeled as a parallel combination of an OR gate and a NOR gate. There are thus six independent nodes to be considered. Table 5 presents the behavior of the device under this fault model.

For further classification and correlation between physical failures and stuck-at fault model, comparison is done between Table 2 with that of the proposed augmented stuck-at fault model output (Table 5). The outcome is presented in column 4 of Table 4, which also lists the faults modeled by the augmented stuck-at fault model. Here, (b_{0}, f_0) indicates that the true output is modeled as b stuck at 0 and complementary output is modeled as f stuck at 0. It can be seen that fault groups $f2$, $f4$, $f9$, $f11$, $f15$, $f16$, $f17$ and $f18$ not modeled by the classical stuck-at fault model, are modeled by the augmented stuck-at fault model. Fault groups $f15$, $f16$ and $f17$ are modeled and are observable at one of the outputs only (True outputs in these cases). Fault groups $f15$, $f16$ and $f17$ exhibit the fault as a complex logical fault. Again, fault groups $f12$ (True output) and $f13$ (Complementary output) are not modeled by the augmented stuck-at fault model. These faults cannot be modeled at the gate level, as the erroneous outputs always appear as undefined values (U) however, the complementary outputs appear as fault free.

A first glance of Table 4 column 4 may give an impression that most of the fault groups in augmented fault model output can only be represented as multiple stuck-at faults. However

Table 4: Correlation between Physical failures vs Stuck-at fault models.

Physical failures vs Stuck-at faults			
Fault groups	*No. of Ph. fls included*	*Corresponding Classical Stuck-at model fault*	*Corresponding Augmented Stuck-at model fault*
$f1$	2	A_0	C_0, E_0
$f2$	1	*Not Covered*	E_0
$f3$	2	B_0	D_0, F_0
$f4$	1	*Not Covered*	F_0
$f5$	8	A_1/B_1	$C_1/D_1/X_1, E_1/F_1/Y_0$
$f6$	4	X_1	$C_1/D_1/X_1, ff$
$f7$	6	X_0	X_0, ff
$f8$	7	Y_0	$ff, E_1/F_1/Y_0$
$f9$	2	*Not Covered*	$C_1/D_1/X_1, Y_1$
$f10$	2	ff	ff
$f11$	6	*Not Covered*	X_0, Y_1
$f12$	1	*Not Covered*	*NotCovered*
$f13$	1	*Not Covered*	*NotCovered*
$f14$	2	Y_1	ff, Y_1
$f15$	1	*Not Covered*	C_1, D_1, X_1 **
$f16$	1	*Not Covered*	C_1, D_1, X_1 **
$f17$	1	*Not Covered*	X_0

ff = *fault-free*, ** = covered by one of the outputs.
No. of Ph. fls. included = Number of Physical failures included.

Table 5: ECL OR/NOR Gate outputs for Proposed Augmented Stuck-at fault model.

ECL OR/NOR Gate Augmented Stuck-at fault model													
Input	ff	C_1	D_1	C_0	D_0	X_1	X_0	E_1	F_1	E_0	F_0	Y_1	Y_0
A B	X	X	X	X	X	X	X	Y	Y	Y	Y	Y	Y
0 0	0	1	1	0	0	1	0	0	0	1	1	1	0
0 1	1	1	1	1	0	1	0	0	0	0	1	1	0
1 0	1	1	1	0	1	1	0	0	0	1	0	1	0
1 1	1	1	1	1	1	1	0	0	0	0	0	1	0

X=OR Output, Y=NOR Output, ff=Fault-free

Figure 8: Two-level implementation of $(A+B)(C+D)$ and $\overline{(A+B)(C+D)}$.

several multiple faults can often be dropped because of equivalence. For example, the multiple fault (c_0, e_0) is equivalent to A_0, which may be covered by the output of the driving logic stuck at 0. The same is true for $f3$ and $f5$. Only the fault groups $f9$, $f11$ and $f18$ are always required to be represented by multiple stuck-at faults.

The multiple stuck-at fault model is an extension of the single stuck fault model, wherein several lines are considered to be simultaneously stuck. If n is denoted to be the number of possible single stuck fault sites, then there are 2^n single stuck faults. Assuming that any multiple stuck fault can occur including the condition of all lines simultaneously stuck, there are $3^n - 1$ possible multiple stuck faults. Assuming that the multiplicity of a fault is no greater than a constant k, then the number of possible multiple stuck faults (F) is given as,

$$F = \sum_{i=1}^{k} \binom{n}{i} 2^i$$

which is usually too large a number to deal explicitly with all multiple faults [21]. For example, the number of multiple faults (double faults, where $k=2$) in a circuit with $n = 1000$ possible fault sites is about 2 million.

Applying multiple stuck at faults to Figure 7 with a multiplicity of faults equal to 2, i.e. double faults, would need 72 multiple faults to be considered, which is obtained by substituting $k=2$ and

$n=10$ in the expression for F. Considering all 72 multiple stuck faults and obtaining a table for all input vectors is too difficult a task. Referring to column 4 of Table 4, we know apriori the behavior of augmented fault model to the 2-level ECL gate. For fault group $f9$, one possibility is to consider the multiple stuck fault of x_1 and y_1 for true and complementary outputs respectively. Similarly, multiple stuck faults need to be considered only for $f11$ and $f18$. Only 3 multiple stuck faults need be considered out of 72 possible double faults since the multiple faults are known apriori from the augmented fault model.

Excluding $f10$, $f12$, $f13$ and $f17$, only about 73.58 % of the physical failures are covered by the classical stuck-at fault model whereas 94.33 % coverage of all detectable faults is obtained using the augmented stuck-at fault model. Even better coverage is obtained if special handling is done for $f15$, $f16$ and $f17$. Test generation and fault simulation would be correct if the complemented output for these cases are assumed to be unknown. In that case 100 % fault coverage of the deterministically testable faults would be obtained. Only 8 single and 3 double stuck-at fault groups need to be considered for modeling all the physical failures of the ECL OR/NOR gate. The proposed augmented stuck-at fault model is also a much simpler and effective fault model compared to the complicated logic model proposed by Morandi et. al. [18], which is obtained using the dictionary for translating circuit elements into a gate level description.

Another possibility is to consider the structure of the fault model shown in figure 6 with multiple stuck at faults which would provide 90.56 % fault coverage. Fault groups $f2$ and $f4$ in this case cannot be included by multiple stuck at faults using the structure shown in Figure 6. The fault coverage obtained would still be less than the fault coverage obtained using the proposed augmented stuck at fault model but the number of nodes need to be considered would be less.

4 Two-level Complex ECL Gates

In this section we extend the fault model developed for 1-level ECL to 2-level ECL OR-AND/NAND and AND/NAND gates.

4.1 Analysis of Physical defects for 2-level ECL OR-AND/NAND Gate

The response of the 2-level ECL OR-AND/NAND gate is evaluated for various faults. The 2-level ECL OR-AND/NAND gate circuit realizing the true function $(A+B).(C+D)$ and its complementary function $\overline{(A+B).(C+D)}$ is used as an example and is shown in Figure 8. Before

Table 6: List of Fault groups vs Physical failures.

ff: Fault-free, $R1/R2/R3/R4/R9$ Open, $D1/D2/D3/D4/R9$ Short, $Q7$ Base to Emitter Short.
$f1$: $Q1$ Emitter/Base Open, $R2$ Short.
$f2$: $Q1$ Collector Open.
$f3$: $Q2$ Emitter/Base Open, $R1$ Short.
$f4$: $Q2$ Collector Open.
$f5$: $Q3$ Emitter/Base Open, $Q7$ Emitter/Base/Collector Open, $R8$ Open, $R9/R10$ Short.
$f6$: $Q3$ Collector Open.
$f7$: $Q4$ Emitter/Base Open, $R4$ Short.
$f8$: $Q4$ Collector Open.
$f9$: $Q5$ Emitter/Base Open, $R13$ Open, $R3$ Short.
$f10$: $Q5$ Collector Open.
$f11$: $Q6/Q10$ Emitter/Base/Collector Open, $R14/R15$ Short.
$f12$: $R14$ Open,$Q8$ Emitter/Base/Collector Open, $R11/Q3$ Base to Collector Short.
$f13$: $Q9$ Emitter/Base/Collector Open, $R6$ Open, $R12/Q9$ Emitter to Base Short.
$f14$: $D1/D2/D3/D4/R10/R15$ Open, $Q3/Q6/Q7/Q10$ Short, $Q10$ Emitter to Base Short, $Q7/Q10$ Base to Collector Short, $R8/R13$ Short.
$f15$: $R5$ Open, $Q1/Q2/Q3$ Emitter to Base Short.
$f16$: $R7$ Open, $Q8$ Emitter to Base Short.
$f17$: $Q9$ Base to Collector Short, $R6/Q9$ Short.
$f18$: $Q10$ Emitter/Base Open, $Q1/Q2$ Short.
$f19$: $Q4/Q5$ Short.
$f20$: $Q4$ Emitter to Base Short.
$f21$: $Q5$ Emitter to Base Short.
$f22$: $Q6$ Emitter to Base Short.
$f23$: $Q1$ Base to Collector Short.
$f24$: $Q2$ Base to Collector Short.
$f25$: $Q4$ Base to Collector Short.
$f26$: $Q5$ Base to Collector Short.
$f27$: $Q8$ Base to Collector Short, $R7/Q8$ Short.
$f28$: $R11$ Open
$f29$: $R12$ Open
$f30$: $R5$ Open

Figure 9: Classical stuck-at fault model for 2-level ECL OR-AND/NAND gate.

performing defect analysis and fault modeling, basic circuit operation, bias conditions, interface constraints have been studied. A list of possible hard failures (opens, shorts etc.) which affect the circuit functionality is given in Table 6. Possible hard failures considered include all possible opens and shorts of transistors, diodes and resistors, transistor junction opens and shorts.

The 2-level ECL OR-AND/NAND gate circuit outputs are obtained after performing SPICE [20] simulations for all input vectors by simulating one failure at a time for all the possible hard failures (opens, shorts etc.) of all the devices (transistors, diodes and resistors). The output of the circuit behavior obtained under various defects are tabulated by combining and grouping the various faults as shown in Table 7.

4.2 Effectiveness of Classical Stuck-at fault model for 2-level Complex ECL OR-AND/NAND Gates

Several gate level implementations are possible for the logic function $(A + B).(C + D)$ and its complement $\overline{(A + B).(C + D)}$. A gate level implementation of the above functions is shown in Figure 9. In order to model the physical failures, the classical stuck-at fault model is applied to the 2-level ECL OR-AND/NAND gate as shown in Figure 9. Results shown in Table 8 were obtained by exercising the model with all possible input combinations for fault-free as well as faulty conditions by introducing one stuck-fault at a time. The defective circuit behavior (Table 7) now can be compared with the classical stuck-at fault model output (Table 8) to obtain the effectiveness of the stuck at model in representing various component failures.

Correlation between 2-level ECL OR-AND/NAND gate classical stuck-at fault model output

Table 7: Circuit behavior under physical failures of 2-level Complex ECL gate (ff=Fault-free, f_1-f_{17}=Defective).

ECL OR/NOR Gate Stuck Open/Short Analysis																
Input	ff	$f1$	$f2$	$f3$	$f4$	$f5$	$f6$	$f7$	$f8$	$f9$	$f10$	$f11$	$f12$	$f13$	$f14$	$f15$
ABCD	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y
0000	0 1	0 1	0 1	0 1	0 1	0 1	1 1	0 1	0 1	0 1	0 1	0 1	0 1	0 0	0 1	1 1
0001	0 1	0 1	0 1	0 1	0 1	1 0	1 1	0 1	0 1	0 1	0 1	0 1	0 1	0 0	0 1	1 1
0010	0 1	0 1	0 1	0 1	0 1	1 0	1 1	0 1	0 1	0 1	0 1	0 1	0 1	0 0	0 1	1 1
0011	0 1	0 1	0 1	0 1	0 1	1 0	1 1	0 1	0 1	0 1	0 1	0 1	0 1	0 0	0 1	1 1
0100	0 1	0 1	1 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	1 1	0 1	0 0	0 1	1 1
0101	1 0	0 1	1 1	1 0	1 0	1 0	1 0	0 1	1 1	1 0	1 0	1 0	0 0	1 0	0 1	1 1
0110	1 0	0 1	1 1	1 0	1 0	1 0	1 0	1 0	1 0	0 1	1 1	1 0	0 0	1 0	0 1	1 1
0111	1 0	0 1	1 1	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	0 0	1 0	0 1	1 1
1000	0 1	0 1	0 1	0 1	1 1	0 1	0 1	0 1	0 1	0 1	0 1	1 1	0 1	0 0	0 1	1 1
1001	1 0	1 0	1 0	0 1	1 1	1 0	1 0	0 1	1 1	1 0	1 0	1 0	0 0	1 0	0 1	1 1
1010	1 0	1 0	1 0	0 1	1 1	1 0	1 0	1 0	1 0	0 1	1 1	1 0	0 0	1 0	0 1	1 1
1011	1 0	1 0	1 0	0 1	1 1	1 0	1 0	1 0	1 0	1 0	1 0	1 0	0 0	1 0	0 1	1 1
1100	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	1 1	0 1	0 0	0 1	1 1
1101	1 0	1 0	1 0	1 0	1 0	1 0	1 0	0 1	1 1	1 0	1 0	1 0	0 0	1 0	0 1	1 1
1110	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	0 1	1 1	1 0	0 0	1 0	0 1	1 1
1111	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	0 0	1 0	0 1	1 1

Input	ff	$f16$	$f17$	$f18$	$f19$	$f20$	$f21$	$f22$	$f23$	$f24$	$f25$	$f26$	$f27$	$f28$	$f29$	$f30$
ABCD	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y
0000	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 0	0 0	1 1	U 1	0 1	0 0
0001	0 1	0 0	0 1	1 0	0 1	0 1	0 0	0 1	0 0	0 0	0 0	0 0	1 1	U 1	0 1	0 0
0010	0 1	0 0	0 1	1 0	0 1	0 0	0 1	0 1	0 0	0 0	0 0	0 0	1 1	U 1	0 1	0 0
0011	0 1	0 0	0 1	1 0	0 1	0 1	0 1	0 1	0 0	0 0	0 0	0 0	1 1	U 1	0 1	0 0
0100	0 1	0 1	0 1	0 1	1 0	0 1	0 1	1 1	1 1	1 1	0 0	0 0	1 1	U 1	0 1	0 0
0101	1 0	0 0	1 1	1 0	1 0	1 1	0 0	1 1	1 1	1 0	1 0	0 0	1 0	1 0	1 U	0 0
0110	1 0	0 0	1 1	1 0	1 0	0 0	1 1	1 1	1 1	1 0	0 0	1 0	1 0	1 0	1 U	0 0
0111	1 0	0 0	1 1	1 0	1 0	1 1	1 1	1 1	1 1	1 0	1 0	1 0	1 0	1 0	1 U	0 0
1000	0 1	0 1	0 1	0 1	1 0	0 1	0 1	1 1	1 1	1 1	0 0	0 0	1 1	U 1	0 1	0 0
1001	1 0	0 0	1 1	1 0	1 0	1 1	0 0	1 1	1 0	1 1	1 0	0 0	1 0	1 0	1 U	0 0
1010	1 0	0 0	1 1	1 0	1 0	0 0	1 1	1 1	1 0	1 1	0 0	1 0	1 0	1 0	1 U	0 0
1011	1 0	0 0	1 1	1 0	1 0	1 1	1 1	1 1	1 0	1 1	1 0	1 0	1 0	1 0	1 U	0 0
1100	0 1	0 1	0 1	0 1	1 0	0 1	0 1	1 1	1 1	1 1	0 0	0 0	1 1	U 1	0 1	0 0
1101	1 0	0 0	1 1	1 0	1 0	1 1	0 0	1 1	1 1	1 1	1 0	0 0	1 0	1 0	1 U	0 0
1110	1 0	0 0	1 1	1 0	1 0	0 0	1 1	1 1	1 1	1 1	0 0	1 0	1 0	1 0	1 U	0 0
1111	1 0	0 0	1 1	1 0	1 0	1 1	1 1	1 1	1 1	1 1	1 0	1 0	1 0	1 0	1 U	0 0

X=OR Output, Y=NOR Output, U=Undefined.

Table 8: ECL 2-level Complex Gate outputs for Classical Stuck-at fault model.

ECL 2-level OR/NOR Gate Classical Stuck-at fault model														
Input	*ff*	A_0	A_1	B_0	B_1	C_0	C_1	D_0	D_1	X_0	X_1	Y_0	Y_1
ABCD	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y
0000	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	1 1	0 0	0 1
0001	0 1	0 1	1 0	0 1	1 0	0 1	0 1	0 1	0 1	0 1	1 1	0 0	0 1
0010	0 1	0 1	1 0	0 1	1 0	0 1	0 1	0 1	0 1	0 1	1 1	0 0	0 1
0011	0 1	0 1	1 0	0 1	1 0	0 1	0 1	0 1	0 1	0 1	1 1	0 0	0 1
0100	0 1	0 1	0 1	0 1	0 1	0 1	1 0	0 1	1 0	0 1	1 1	0 0	0 1
0101	1 0	1 0	1 0	0 1	1 0	1 0	1 0	0 1	1 0	0 0	1 0	1 0	1 1
0110	1 0	1 0	1 0	0 1	1 0	0 1	1 0	1 0	1 0	0 0	1 0	1 0	1 1
0111	1 0	1 0	1 0	0 1	1 0	1 0	1 0	1 0	1 0	0 0	1 0	1 0	1 1
1000	0 1	0 1	0 1	0 1	0 1	0 1	1 0	0 1	1 0	0 1	1 1	0 0	0 1
1001	1 0	0 1	1 0	1 0	1 0	1 0	1 0	0 1	1 0	0 0	1 0	1 0	1 1
1010	1 0	0 1	1 0	1 0	1 0	0 1	1 0	1 0	1 0	0 0	1 0	1 0	1 1
1011	1 0	0 1	1 0	1 0	1 0	1 0	1 0	1 0	1 0	0 0	1 0	1 0	1 1
1100	0 1	0 1	0 1	0 1	0 1	0 1	1 0	0 1	1 0	0 1	1 1	0 0	0 1
1101	1 0	1 0	1 0	1 0	1 0	1 0	1 0	0 1	1 0	0 0	1 0	1 0	1 1
1110	1 0	1 0	1 0	1 0	1 0	0 1	1 0	1 0	1 0	0 0	1 0	1 0	1 1
1111	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	0 0	1 0	1 0	1 1

X=OR Output, Y=NOR Output.

and physical failures is shown in columns 1-3 of Table 9, where it can be seen that almost all the classical stuck-at faults model some physical failures. The physical failures as modeled by fault-groups $f1$, $f3$, $f5$, $f7$, $f9$, $f12$, $f13$, $f17$, $f18$, $f19$ and $f27$ are modeled accurately using the classical stuck-at fault model. The faults $f28$ and $f29$ cause one of the outputs to become indeterminate, which cannot be represented by a logical fault model. From the remaining, the classical stuck-at fault model leaves 17 fault groups uncovered out of 28 detectable fault groups, corresponding to 40 physical failures out of 76 possible hard failures examined. Only 39.28 % fault groups are covered using the classical stuck-at fault model corresponding to 47.36 % of physical failures. In the next section, we present an augmented stuck-at fault model that provides a higher coverage of physical failures compared to the classical stuck-at fault model.

4.3 An Augmented Stuck-at fault model for 2-level ECL OR-AND/NAND Gates

The classical input/output stuck-at fault model is not effective for modeling ECL gates. Figure 10 shows the proposed augmented stuck-at fault model which improves the fault coverage. Here, the device is modeled as a parallel combination of OR-AND and OR-NAND gates realizing the true

Figure 10: Proposed augmented stuck-at fault model.

and complementary function. Thus, there are 10 independent nodes to be considered. Table 10 10 presents the behavior of the device under this fault model.

For further classification and correlation between physical failures and stuck-at fault model, comparison is done between Table 7 with that of the proposed augmented stuck-at fault model output (Table 10). The outcome is presented in column 4 of Table 9, which also lists the faults modeled by the augmented stuck-at fault model. The fault groups $f2$, $f4$, $f6$, $f8$, $f10$, $f11$, $f14$, $f15$, $f16$, $f20$, $f21$, $f22$, $f23$, $f24$, $f25$ $f26$ and $f30$ not modeled by the classical stuck-at fault model, are modeled by the augmented stuck-at fault model. Fault groups $f2$, $f4$, $f20$, $f21$, $f23$ and $f24$ are modeled and are observable at one of the outputs only. For these fault groups, the other output exhibits the fault as a complex logical fault. Fault groups $f28$ (True output) and $f29$ (Complementary output) cannot be modeled at the gate level, as the erroneous outputs always appear as undefined values (U), however, the complementary outputs appear as fault free.

Fault groups ($f2$, $f4$, $f20$, $f21$, $f23$ and $f24$) which are modeled and observable at one of the outputs according to the model works effectively when a 2-level ECL OR-AND/NAND gate alone is modeled. Abnormal behavior may be observed on the other output which is not modeled properly and might lead to fault masking when the outputs reconverge on a subsequent gate. A first glance of Table 9 column 4 may give an impression that most of the fault groups in augmented fault model are modeled as multiple faults (double faults). However, several multiple faults can be dropped because of equivalence, for example, the multiple fault (b $_0$, f_0) modeled by fault group $f1$ is equivalent to B $_0$, which may be covered by the output of the driving logic stuck at 0. Only

Table 9: Correlation between Physical failures vs Stuck-at fault models for 2-level Complex ECL Gate.

Physical failures vs Stuck-at faults			
Fault groups	*No. of Ph. fls included*	*Corresponding Classical Stuck-at model fault*	*Corresponding Augmented Stuck-at model fault True o/p , Comp. o/p*
$f1$	2	B_0	b_0 , f_0
$f2$	1	*Not Covered*	- , f_0 **
$f3$	2	A_0	a_0 , e_0
$f4$	1	*Not Covered*	- , e_0 **
$f5$	6	A_1/B_1	a_1/b_1 , e_1/f_1
$f6$	1	*Not Covered*	- , ff
$f7$	2	D_0	d_0 , h_0
$f8$	1	*Not Covered*	ff , h_0
$f9$	3	C_0	c_0 , g_0
$f10$	1	*Not Covered*	ff , g_0
$f11$	6	*Not Covered*	c_1/d_1 , ff
$f12$	5	X_0	x_0 , ff
$f13$	5	Y_0	ff , y_0
$f14$	15	*Not Covered*	x_0 , y_1 †
$f15$	4	*Not Covered*	x_1 , y_1 †
$f16$	2	*Not Covered*	x_0 , e_1/f_1 †
$f17$	3	Y_1	ff , y_1
$f18$	3	A_1/B_1	a_1/b_1 , e_1/f_1
$f19$	2	C_1/D_1	c_1/d_1 , g_1/h_1
$f20$	1	*Not Covered*	c_0 , - **
$f21$	1	*Not Covered*	d_0 , - **
$f22$	1	*Not Covered*	c_1/d_1 , y_1 †
$f23$	1	*Not Covered*	c_1/d_1 , - **
$f24$	1	*Not Covered*	c_1/d_1 , - **
$f25$	1	*Not Covered*	c_0 , y_0 †
$f26$	1	*Not Covered*	d_0 , y_0 †
$f27$	3	X_1	x_1 , ff
$f28$	1	@	@ , ff
$f29$	1	@	ff , @
$f30$	1	*Not Covered*	x_0 , y_0 †

ff = *fault-free*, ** = observable at one of the outputs.
@ = cannot be modeled at gate level. † = multiple stuck-at fault.
No. of Ph. fls. included = Number of Physical failures included.
- = too complex to be modeled at gate level.

Table 10: ECL 2-level Complex Gate outputs for Proposed Augmented Stuck-at fault model.

ECL 2-level OR/NOR Gate Augmented Stuck-at fault model																						
Input	ff	ff	a_0	a_1	b_0	b_1	c_0	c_1	d_0	d_1	e_0	e_1	f_0	f_1	g_0	g_1	h_0	h_1	x_0	x_1	y_0	y_1
ABCD	X	Y	X	X	X	X	X	X	X	X	Y	Y	Y	Y	Y	Y	Y	Y	X	X	Y	Y
0000	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	1
0001	0	1	0	1	0	1	0	0	0	0	1	0	1	0	1	1	1	1	0	1	0	1
0010	0	1	0	1	0	1	0	0	0	0	1	0	1	0	1	1	1	1	0	1	0	1
0011	0	1	0	1	0	1	0	0	0	0	1	0	1	0	1	1	1	1	0	1	0	1
0100	0	1	0	0	0	0	0	1	0	1	1	1	1	1	1	0	1	0	0	1	0	1
0101	1	0	1	1	0	1	1	1	0	1	0	0	1	0	0	0	1	0	0	1	0	1
0110	1	0	1	1	0	1	0	1	1	1	0	0	1	0	1	0	0	0	0	1	0	1
0111	1	0	1	1	0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	1	0	1
1000	0	1	0	0	0	0	0	1	0	1	1	1	1	1	1	0	1	0	0	1	0	1
1001	1	0	0	1	1	1	1	1	0	1	1	0	0	0	0	0	1	0	0	1	0	1
1010	1	0	0	1	1	1	0	1	1	1	1	0	0	0	1	0	0	0	0	1	0	1
1011	1	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	1
1100	0	1	0	0	0	0	0	1	0	1	1	1	1	1	1	0	1	0	0	1	0	1
1101	1	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	1	0	0	1	0	1
1110	1	0	1	1	1	1	0	1	1	1	0	0	0	0	1	0	0	0	0	1	0	1
1111	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	1

X=OR Output, Y=NOR Output.

the fault groups $f14$, $f15$, $f16$, $f22$, $f25$, $f26$ and $f30$ are always required to be represented by multiple stuck at faults.

Applying multiple stuck at faults to Figure 9 with a multiplicity of faults equal to 2, i.e. double faults, would need 198 multiple faults to be considered, which is obtained by substituting $k=2$ and $n=10$ in the expression for F. Considering all 198 multiple stuck faults and obtaining a table for all input vectors is too difficult a task. Referring to column 4 of Table 9, we know apriori the behavior of augmented fault model to the 2-level ECL OR-AND/NAND gate. For fault group $f14$, we need to consider the multiple stuck fault of x_0 and y_1 for true and complementary outputs. Similarly, multiple stuck faults need to be considered only for $f15$, $f16$, $f22$, $f25$, $f26$ and $f30$. Only 7 multiple stuck faults need be considered out of 198 possible double faults since the multiple faults are known apriori from the augmented fault model.

90.78 % coverage of all detectable faults is obtained by the augmented stuck-at fault model compared to 47.36 % coverage obtained using the classical stuck-at fault model. Even better coverage is obtained if special handling is done for $f2$, $f4$, $f20$, $f21$, $f23$ and $f24$. Test generation and fault simulation would be correct if the complemented outputs for these cases are assumed to be unknown. In that case 100 % fault coverage of the deterministically testable faults would

Figure 11: ECL AND/NAND gate.

be obtained. Only 14 single and 7 double stuck-at faults need be considered for modeling all the physical failures of the 2-level ECL gate investigated. It can be seen that the augmented fault model proposed for 2-level ECL gates is much simpler and effective compared to the logic model proposed by Morandi et. al. [18].

Another possibility is to consider the structure of the fault model shown in figure 9 with multiple stuck at faults which would provide 68.42 % fault coverage. Fault groups $f8$, $f10$, $f11$, $f12$, $f13$, $f17$ and $f27$ in this case cannot be included by multiple stuck at faults using the structure shown in Figure 9. The fault coverage obtained would still be less than the fault coverage obtained using the proposed augmented stuck at fault model but the number of nodes to be considered would be less.

4.4 Analysis of Physical defects for 2-level ECL AND/NAND Gate

The response of the 2-level ECL AND/NAND gate is evaluated for various faults. The 2-level ECL AND/NAND gate circuit realizing the true function $(A.B)$ and its complementary function $\overline{(A.B)}$ is used as an example and is shown in Figure 11. Before performing defect analysis and fault modeling, basic circuit operation, bias conditions, interface constraints have been studied. A list of possible hard failures (opens, shorts etc.) which affect the circuit functionality is given in Table 11. Possible hard failures considered include all possible opens and shorts of transistors,

Table 11: List of Fault groups vs Physical failures for 2-level ECL AND/NAND.

ff: Fault-free, $R1/R2/R9$ Open, $D1/D2/D3/D4$ Short,
$Q7$ Base to Emitter Short.
$f1$: $Q1$ Collector Open, $Q6$ Base to Emitter Short.
$f2$: $Q1/Q4$ Base/Emitter Open, $D1/D2/R10/D3/D4/R15$ Open
$R8/R13/Q3/Q6/Q7/Q10$ Short, $Q7$ Base to Collector Short
$Q10$ Base to Emitter & Base to Collector Short
$f3$: $Q4$ Collector Open, $R6/Q9$ Short, $Q4$ Base to Emitter Short.
$f4$: $R5$ Open, $Q1$ Base to Emitter Short, $Q3$ Base to Emitter Short.
$f5$: $R6$ Open, $Q4$ Base to Collector Short, $Q9$ Base to Emitter Short,
$Q9$ Emitter/Base/Collector Open, $R12$ Short.
$f6$: $R7$ Open.
$f7$: $R8$ Open, $R9/R10$ Short, $Q3$ Emitter/Base Open,
$Q7$ Collector/Base/Emitter Open, $Q1$ Short.
$f8$: $R11$ Open.
$f9$: $R12$ Open.
$f10$: $R13$ Open, $R14/R15$ Short, $Q6$ Collector/Base/Emitter Open
$Q10$ Collector/Base/Emitter Open.
$f11$: $R14$ Open, $R11$ Short, $Q3/Q6$ Base to Collector Short.
$Q8$ Collector/Base/Emitter Open.
$f12$: $R5$ Short.
$f13$: $R7/Q8$ Short, $Q8$ Base to Collector Short.
$f14$: $Q4$ Short.
$f15$: $Q1$ Base to Collector Short.
$f16$: $Q8$ Emitter to Base Short.
$f17$: $Q9$ Base to Collector Short.
$f18$: $Q3$ Collector Open.

diodes and resistors, transistor junction opens and shorts.

The 2-level ECL AND/NAND gate circuit outputs are obtained after performing SPICE[20] simulations for all input vectors by simulating one failure at a time for all the possible hard failures (opens, shorts etc.) of all the devices (transistors, diodes and resistors). The output of the circuit behavior obtained under various defects are tabulated by combining and grouping the various faults as shown in Table 12.

4.5 Effectiveness of Classical Stuck-at fault model for 2-level Complex ECL AND/NAND Gates

Gate level implementation of the above functions is shown in Figure 12. In order to model the physical failures, the classical stuck-at fault model is applied to the 2-level ECL AND/NAND gate as shown in Figure 12. Results shown in Table 13 were obtained by exercising the model with all possible input combinations for fault-free as well as faulty conditions by introducing one

Figure 12: Classical stuck-at fault model.

stuck-fault at a time. The defective circuit behavior (Table 12) now can be compared with the classical stuck-at fault model output (Table 13) to obtain the effectiveness of the stuck at model in representing various component failures.

Correlation between 2-level ECL AND/NAND gate classical stuck-at fault model output and physical failures is shown in columns 1-3 of Table 14, where it can be seen that almost all the classical stuck-at faults model some physical failures. The physical failures as modeled by fault-groups $f2$, $f3$, $f5$, $f7$, $f11$, $f13$, and $f14$ are modeled accurately using the classical stuck-at fault model. The faults $f8$ and $f9$ cause one of the outputs to become indeterminate, which cannot be represented by a logical fault model. From the remaining, the classical stuck-at fault model leaves 11 fault groups uncovered out of 16 detectable fault groups, corresponding to 20 physical failures out of 70 possible hard failures examined. Only 39.28 % fault groups are covered using the classical stuck-at fault model corresponding to 47.36 % of physical failures. In the next section, we present an augmented stuck-at fault model that provides a higher coverage of physical failures compared to the classical stuck-at fault model.

4.6 An Augmented Stuck-at fault model for 2-level ECL AND/NAND Gates

The classical input/output stuck-at fault model is not effective for modeling ECL gates. Figure 13 shows the proposed augmented stuck-at fault model which improves the fault coverage. Here, the device is modeled as a parallel combination of OR-AND and OR-NAND gates realizing the true and complementary function. Thus, there are 10 independent nodes to be considered. Table 15 presents the behavior of the device under this fault model.

For further classification and correlation between physical failures and stuck-at fault model, comparison is done between Table 12 with that of the proposed augmented stuck-at fault model

Figure 13: Proposed augmented stuck-at fault model.

Table 14: Correlation between Physical failures vs Stuck-at fault models for 2-level Complex ECL AND/NAND Gate.

Physical failures vs Stuck-at faults			
Fault groups	*No. of Ph. fls included*	*Corresponding Classical Stuck-at model fault*	*Corresponding Augmented Stuck-at model fault True o/p , Comp. o/p*
$f1$	2	*Not Covered*	b_1 , d_0/Y_1 †
$f2$	19	A_0/B_0	$a_0/b_0/X_0$, d_0/Y_1
$f3$	4	Y_1	ff , d_0/Y_1
$f4$	3	*Not Covered*	X_1 , d_0/Y_1 †
$f5$	7	Y_0	ff , c_0/Y_0
$f6$	1	*Not Covered*	$a_0/b_0/X_0$, c_1 †
$f7$	9	A_1	a_1 , c_1
$f8$	1	@	@ ff
$f9$	1	@	ff @
$f10$	9	*Not Covered*	b_1 , ff
$f11$	7	X_0	$a_0/b_0/X_0$, ff
$f12$	1	*Not Covered*	$a_0/b_0/X_0$, - **
$f13$	3	X_1	X_1 , ff
$f14$	1	B_1	b_1 , d_1
$f15$	1	*Not Covered*	b_1 , - **
$f16$	1	*Not Covered*	$a_0/b_0/X_0$, c_1 †
$f17$	1	*Not Covered*	X_1 , ff
$f18$	1	*Not Covered*	- , ff

ff = *fault-free*, ** = observable at one of the outputs.
@ = cannot be modeled at gate level. † = multiple stuck-at fault.
No. of Ph. fls. included = Number of Physical failures included.
- = too complex to be modeled at gate level.

Table 15: ECL 2-level Complex Gate outputs for Proposed Augmented Stuck-at fault model.

Augmented Stuck-at fault model														
Input	ff	ff	a_0	a_1	b_0	b_1	c_0	c_1	d_0	d_1	x_0	x_1	y_0	y_1
AB	X	Y	X	X	X	X	Y	Y	Y	Y	X	X	Y	Y
00	0	1	0	0	0	0	0	1	1	1	0	1	0	1
01	0	1	0	1	0	0	0	0	1	1	0	1	0	1
10	0	1	0	0	0	1	0	1	1	0	0	1	0	1
11	1	0	0	1	0	1	0	0	1	0	0	1	0	1

X=OR Output, Y=NOR Output.

output (Table 15). The outcome is presented in column 4 of Table 14, which also lists the faults modeled by the augmented stuck-at fault model. The fault groups $f2$, $f4$, $f6$, $f8$, $f10$, $f11$, $f14$, $f15$, $f16$, $f20$, $f21$, $f22$, $f23$, $f24$, $f25$ $f26$ and $f30$ not modeled by the classical stuck-at fault model, are modeled by the augmented stuck-at fault model. Fault groups $f2$, $f4$, $f20$, $f21$, $f23$ and $f24$ are modeled and are observable at one of the outputs only. For these fault groups, the other output exhibits the fault as a complex logical fault. Fault groups $f28$ (True output) and $f29$ (Complementary output) cannot be modeled at the gate level, as the erroneous outputs always appear as undefined values (U), however, the complementary outputs appear as fault free.

Fault groups ($f2$, $f4$, $f20$, $f21$, $f23$ and $f24$) which are modeled and observable at one of the outputs according to the model works effectively when a 2-level ECL AND/NAND gate alone is modeled. Abnormal behavior may be observed on the other output which is not modeled properly and might lead to fault masking when the outputs reconverge on a subsequent gate. A first glance of Table 14 column 4 may give an impression that most of the fault groups in augmented fault model are modeled as multiple faults (double faults). However, several multiple faults can be dropped because of equivalence, for example, the multiple fault (b $_0$, f_0) modeled by fault group $f1$ is equivalent to B $_0$, which may be covered by the output of the driving logic stuck at 0. Only the fault groups $f14$, $f15$, $f16$, $f22$, $f25$, $f26$ and $f30$ are always required to be represented by multiple stuck at faults.

Applying multiple stuck at faults to Figure 12 with a multiplicity of faults equal to 2, i.e. double faults, would need 198 multiple faults to be considered, which is obtained by substituting k=2 and n=10 in the expression for F. Considering all 198 multiple stuck faults and obtaining a table for all input vectors is too difficult a task. Referring to column 4 of Table 14, we know apriori the behavior of augmented fault model to the 2-level ECL AND/NAND gate. For fault

group $f14$, we need to consider the multiple stuck fault of x_0 and y_1 for true and complementary outputs. Similarly, multiple stuck faults need to be considered only for $f15$, $f16$, $f22$, $f25$, $f26$ and $f30$. Only 7 multiple stuck faults need be considered out of 198 possible double faults since the multiple faults are known apriori from the augmented fault model.

90.78 % coverage of all detectable faults is obtained by the augmented stuck-at fault model compared to 47.36 % coverage obtained using the classical stuck-at fault model. Even better coverage is obtained if special handling is done for $f2$, $f4$, $f20$, $f21$, $f23$ and $f24$. Test generation and fault simulation would be correct if the complemented outputs for these cases are assumed to be unknown. In that case 100 % fault coverage of the deterministically testable faults would be obtained. Only 14 single and 7 double stuck-at faults need be considered for modeling all the physical failures of the 2-level ECL gate investigated. It can be seen that the augmented fault model proposed for 2-level ECL gates is much simpler and effective compared to the logic model proposed by Morandi et. al. [18].

Another possibility is to consider the structure of the fault model shown in figure 9 with multiple stuck at faults which would provide 68.42 % fault coverage. Fault groups $f8$, $f10$, $f11$, $f12$, $f13$, $f17$ and $f27$ in this case cannot be included by multiple stuck at faults using the structure shown in Figure 12. The fault coverage obtained would still be less than the fault coverage obtained using the proposed augmented stuck at fault model but the number of nodes to be considered would be less.

5 Power Supply Current Monitoring

Certain defects during manufacturing process, such as, spot defects in lithography or in any of the processing steps could lead to a short. Current testing has been studied [22, 23] to be a potential methodology for detecting such shorts in CMOS devices.

ECL circuits draw almost constant power supply current, independent of frequency [1]. It can be observed from the structure of ECL that when the input transistors are OFF, the other differential transistor will be ON and vice-versa. Certain defects could manifest itself in drawing excessive power supply current and such defects can be detected using power supply current monitoring. SPICE simulations for fault R_5 shorted indicates that the current drawn under fault is almost 100 times that of fault-free. However, certain faults such as, shorts in the differential input transistors do not manifest itself in drawing excessive power supply current as shorting causes the other differential transistor (Q_3/Q_6) to turn OFF. This happens as the voltage at

Figure 14: Current drawn by an ECL gate under R_{5} short and fault-free.

the common emitter point rises due to the short and since the base of the fixed bias transistors (Q_3/Q_6) are held constant, these transistors cannot turn ON. Figure 14 shows current drawn by an ECL OR/NOR gate under fault-free and faulty conditions.

6 Design for Testability

Careful observation of Tables 2, 7 and 12 indicate that for some of the physical failures, the input test vectors cause both the true and complementary outputs to exhibit erroneous $LIKE$ outputs (i.e. similar outputs, 00 or 11) instead of the true and complementary outputs exhibiting fault-free $UNLIKE$ outputs (i.e. 01 or 10). Out of the 18 classified faults for various physical failures of devices for the ECL OR/NOR gate, 7 of the fault groups exhibit erroneous $LIKE$ outputs with at least one or more input vectors, which is approximately 39 % and out of the 30 classified fault groups for the 2-level ECL gate, 20 of them exhibit erroneous $LIKE$ outputs which is approximately 66.66 %. By using the following simple design for testability approach, it is possible to ON-LINE detect such faults. This may be useful in fault-tolerant systems.

The design for testability approach uses an exclusive-OR gate connected to the output of the ECL gate as shown in Figure 15, with the output of the exclusive-OR gate termed as the $\overline{ERROR}$ signal. When the true and complementary outputs of the ECL gate is fault-free $UNLIKE$ output (i.e. 01 or 10), then the $\overline{ERROR}$ signal would be a 1 indicating that $\overline{ERROR}$=1 and $ERROR$=0

Figure 16: Exclusive-NOR gate to detect LIKE errors in interconnect modules.

(i.e. $NO\ ERROR$). Whenever any of the faults cause the outputs of the gate to exhibit erroneous $LIKE$ outputs (i.e. 00 or 11), then the $\overline{ERROR}$ signal would become a 0 indicating that $\overline{ERROR}$=0 and $ERROR$=1 (i.e. an $ERROR$ has occurred). Use of an Exclusive-OR or NOR to detect $LIKE$ errors in single level ECL gates would be an increase in area overhead and might be prohibitive. However, if the gate is multiple level and sufficiently complex, then the overhead may be justifiable in some situations. This approach may be effective at module level, at the end of high speed data bus, in clock chains etc. and in other applications where there is probability of $LIKE$ errors to occur.

This design for testability approach is not only useful for ECL gates but can be used in applications where true and complementary signals are being simultaneously transmitted between one unit to the other or while driving long distances using twisted pairs or any other mode of communication. The output driver gate could exhibit erroneous $LIKE$ output under faults or if the communication channel develops snag with an open or short between the true and complementary lines, the receive end would exhibit erroneous $LIKE$ error condition. Figure

16 shows an implementation of the design for testability approach using an exclusive-NOR gate in a general line-driving application, where under erroneous $LIKE$ output conditions the $ERROR$ signal would be a 1 and would be a 0 for fault-free $UNLIKE$ output conditions.

7 Conclusions

The effectiveness of the classical stuck-at fault model in modeling physical failures that are possible in a one and two-level ECL gates have been examined. An augmented stuck-at fault model has been proposed as the classical stuck-at fault model did not model a major fraction of the physical failures. High fault coverage can be obtained using the augmented stuck-at fault model for both one-level and two-level ECL gates compared to the classical stuck-at fault model. The augmented stuck-at fault model can easily be extended to multi-level complex ECL gates. A design for testability approach was presented for detecting $LIKE$ error conditions occurring in gates with true and complementary outputs which is a normal implementation for ECL logic devices. The design for testability approach presented here can also be used for detecting $LIKE$ error conditions in applications where true and complementary signals are transmitted from one unit to the other or while signals are driven long distances using twisted pairs or other modes of communications.

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