1) What is the range of values for the PC offset for the following instructions: JMP, LEA, STI?

2) What information is stored in the Processor State Register? What bit locations hold this information?

3) What does the JMP R2 instruction do? How is this different from the RET instruction?

4) What is PC offset for the following BR instruction? Now show the 16 bits that make up the BR instruction.

   BRz data1
   ADD R2, R2, #5
   JSRR R4
   data1 .FILL 0x1234

5) Given the following information what will be the value in the PC after the following instruction TRAP x23, What is the first instruction executed by the TRAP routine?

<table>
<thead>
<tr>
<th>location</th>
<th>data</th>
<th>location</th>
<th>data</th>
<th>location</th>
<th>data</th>
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<tbody>
<tr>
<td>x0020</td>
<td>x0420</td>
<td>x0230</td>
<td>x2A43</td>
<td>x0323</td>
<td>xFADC</td>
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<td>x0021</td>
<td>x0251</td>
<td>x0231</td>
<td>x32AC</td>
<td>x0324</td>
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<td>x0022</td>
<td>x046C</td>
<td>x0232</td>
<td>x5E1F</td>
<td>x0325</td>
<td>xAE1F</td>
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<td>x0326</td>
<td>x0233</td>
<td>x8FB2</td>
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<td>x0234</td>
<td>xE8A1</td>
<td>x0327</td>
<td>x98A1</td>
</tr>
</tbody>
</table>

6) What change signifies that the keyboard is in interrupt vs polling mode?

7) What is the difference between the frame pointer and the stack pointer?

8) List the 10 parts on the stack protocol in order. What parts have to be done by the caller or callee, and what parts were a choice made by the protocol designer?

9) What do the following instructions have in common? LDI, LDR, STI, STR, JSRR, JMP, RET

10) What instructions make up a PUSH? What instructions make up a POP?

11) If the LC3 had 32 registers how would the ADD instruction be affected?

12) How many times does the LDR instruction access memory? What about STI? What about TRAP?

13) What is the purpose of bit 15 in the KBSR? Bit 14?

14) Besides an interrupt signal what else does the interrupting device need to send the LC3 processor for an interrupt to be handled?