

- 1) How many 64 bit floating point numbers can be stored in a 16 byte cache block? 64 byte cache block?

2, 8

- 2)

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for(i = 0; i < 8; i++)
  for(j = 0; j < 1000; j++)
    A[i][j] = B[i][0] + A[i][j];
```

- a. In the C code segment above what variable references exhibit temporal locality?

B[i][0]

- b. What variable references exhibit spatial locality?

A[i][j]

- 3) Given the following information for a direct-mapped cache design with 32 bit address, 4 byte words and byte addressing:

Tag	Index	Offset
31-13	12-6	5-0

- a) How many words are in a block/cache line?

6 bits of Offset, so cache line is 2^6 bytes, 4bytes per word so 16 words per cache line

- b) How many blocks/cache lines are in the cache?

7 bits of Index, so 2^7 or 128 cache lines

- c) How many bits of data can the cache store?

2^7 lines * 2^6 bytes/line * 8 bits/byte = 65536 bits

- d) How many bits are used per cache line to manage the cache (valid bit plus tag bits)?

19 tag bits + 1 valid bit = 20 bits per line

- e) How many bits are used overall to manage the cache (valid bits plus tag bits)?

20 bits * 2^7 lines = 2560 bits

- f) What is the total number of bits the cache requires for storage and management?

65536 bits + 2560 bits = 68096 bits

4) Given the following information calculate the average memory access time(AMAT).

$$\text{AMAT} = \text{HitTime} + \text{MissRatio} * \text{MissPenalty}$$

- L1 miss rate 5%.
- L1 access time 5 cycles
- Memory access time 150 cycles

What would the L1 miss rate need to be to achieve a AMAT of 6 cycles?

$$5 + (\text{MR} * 150) = 6 \quad // \text{ Subtract 5 from both sides}$$

$$\text{MR} * 150 = 1 \quad // \text{ Divide both sides by 150}$$

$$\text{MR} = 1/150 \text{ or } 0.6\% \text{ miss rate}$$