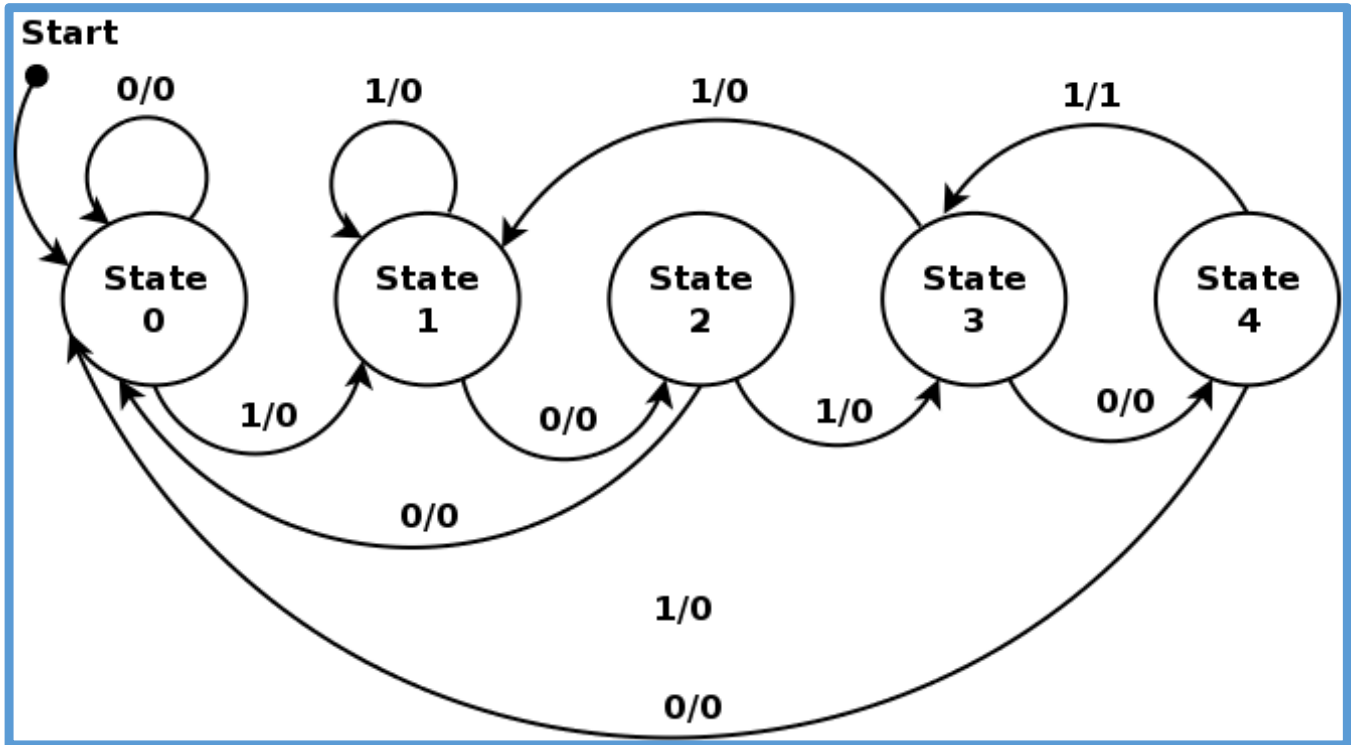


CS270 Homework Assignment 3 (H3)

Due week of Apr. 25, will be graded during lab, no late submissions.
Homework and programming assignments are to be done individually.

Instructions: Design a Logisim circuit that implements the state machine shown below:



Here are a few clarifications that may help you, and questions you should be able to answer:

- What is the sequence of bits that is detected by this state machine?
- State should be stored in D-latches, how many do you need?
- The truth table is combinational logic similar to what you have already done.
- You must use a D-latch the output, since it's on a transition.
- Optimization is allowed and encouraged, the fewer gates the better!
- Why are there only 10 rows in the truth table instead of $2^4 = 16$?

| <i>Current State</i> | <i>Input</i> | <i>Output</i> | <i>Next State</i> |
|----------------------|--------------|---------------|-------------------|
| <i>000</i> | <i>0</i> | <i>0</i> | <i>000</i> |
| <i>000</i> | <i>1</i> | <i>0</i> | <i>001</i> |
| <i>001</i> | <i>0</i> | | |
| <i>001</i> | <i>1</i> | | |
| <i>010</i> | <i>0</i> | | |
| <i>010</i> | <i>1</i> | | |
| <i>011</i> | <i>0</i> | | |
| <i>011</i> | <i>1</i> | | |
| <i>100</i> | <i>0</i> | | |
| <i>100</i> | <i>1</i> | | |

Create a Logisim circuit called H3.circ and turn it in to the Canvas drop box. You will be asked about your circuit at your recitation during the week of April 25.