CS370 Operating Systems
Colorado State University
Yashwant K Malaiya
Spring 2021

Slides based on
- Text by Silberschatz, Galvin, Gagne
- Various sources
CS370: Operating Systems  
[Spring 2021 Website in progress]

CS370 Web site: https://www.cs.colostate.edu/~cs370

To be revised for Spring 2021.

Announcements: Course Objectives:
CS370 is a core undergraduate CS course. The objective of this course is to understand the broad range of issues that underlie the modern Operating Systems. We focus on key concepts and algorithms that are used in both commercial and open-source operating systems. This course will cover the following broad areas:

1. Operating systems - perspective, terminology, structure.
2. Processes, threads, concurrency and deadlocks
3. CPU Scheduling algorithms
4. Deadlocks and resource management
5. Memory - address translation and virtual memory
6. Storage architecture and File System
7. Virtual Machines and data centers

We may discuss advanced topics (security and reliability) and recent development based on time available.

Lecture Coordinates
Sec 1: MS Teams Ch S1, Tu, Th 9:30-10:45 AM
Sec 2: MS Teams Ch S2, Tu, Th 12:30 - 1:45 PM
Sec 801: MS Teams Ch S2

Help Sessions
To be announced
Expand email abbreviation: C.E = colostate.edu

Instructors
Yashwant Malaiya
Office: Room CSB 356 (not in Spring)
Office Hours: 3:30-4:30 PM on Mon, Wed (Tent on Teams, email to arrange)
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Teaching Assistants
Graduate TA: Richi Rodriguez
Richi.Rodriguez at C.E
CSB 120: Hours: Wed, Fri 3-4 PM

Undergraduate TA: Xinyi Wang
xinyi99 at C.E
CSB 120 Hours: Tues, Thurs 4-5 PM

Phil Sharp
Office Hours:
2-3 PM on Tues, Thurs.
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Graduate TA: Mohit Kumar Katragadda
MohitKumar.Katragadda at C.E
CSB 120 Hours: Mon, Sat 2-3 PM

Undergraduate TA: Anteneh Zeleke
Anteneh.Zeleke at rams.C.E
CSB 120 Hours: Mon. 3-5 PM

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Operating Systems

• Part 1: How to do things
  – concurrently/in parallel

• Part 2: How to find stuff
  – Information in a many layered memory system

• Continued technological evolution
  – Techniques and challenges will evolve
  – Very high performance and capacity needed for modern applications: AI, Big Data
Technology Trends: Moore’s Law

Gordon Moore (co-founder of Intel) predicted in 1965 that the transistor density of semiconductor chips would double roughly every 18 months.

2X transistors/Chip Every 1.5 years
Called “Moore’s Law”

Microprocessors have become smaller, denser, and more powerful.

Moore’s law is dead? / not dead?

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Moore’s Law: The number of transistors on microchips doubles every two years.

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important for other aspects of technological progress in computing – such as processing speed or the price of computers.

Transistor count

50,000,000,000
10,000,000,000
5,000,000,000
1,000,000,000
500,000,000
100,000,000
50,000,000
10,000,000
5,000,000
1,000,000
500,000
100,000
50,000
10,000
5,000
1,000

Year in which the microchip was first introduced

Data source: Wikipedia (wikipedia.org/wiki/Transistor_count)

OurWorldInData.org – Research and data to make progress against the world’s largest problems.

Licensed under CC-BY by the authors Hannah Ritchie and Max Roser.
## Computer Performance Over Time

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Uniprocessor speed (MIPS)</td>
<td>1</td>
<td>200</td>
<td>2500</td>
<td>2.5K</td>
</tr>
<tr>
<td>CPUs per computer</td>
<td>1</td>
<td>1</td>
<td>10+</td>
<td>10+</td>
</tr>
<tr>
<td>Processor MIPS/($)</td>
<td>$100K</td>
<td>$25</td>
<td>$0.20</td>
<td>500K</td>
</tr>
<tr>
<td>DRAM Capacity (MiB)/$</td>
<td>0.002</td>
<td>2</td>
<td>1K</td>
<td>500K</td>
</tr>
<tr>
<td>Disk Capacity (GiB)/$</td>
<td>0.003</td>
<td>7</td>
<td>25K</td>
<td>10M</td>
</tr>
<tr>
<td>Home Internet</td>
<td>300 bps</td>
<td>256 Kbps</td>
<td>20 Mbps</td>
<td>100K</td>
</tr>
<tr>
<td>Machine room network</td>
<td>10 Mbps (shared)</td>
<td>100 Mbps (switched)</td>
<td>10 Gbps (switched)</td>
<td>1000</td>
</tr>
<tr>
<td>Ratio of users to computers</td>
<td>100:1</td>
<td>1:1</td>
<td>1:several</td>
<td>100+</td>
</tr>
</tbody>
</table>

Anderson Dahlin 2014
Storage Capacity

- Retail hard disk capacity in GB
Course Resources

• Microsoft Teams
  – Lectures, interaction, announcements

• Canvas: Assignments, quizzes, submission, grades

• Webpage http://www.cs.colostate.edu/~cs370
  – Home: Overview, contacts
  – Syllabus: Grading, Text, Responsibilities, Policies, Conduct
  – Schedule: Key dates, weekly schedules, slides, assignments, readings

ABOUT ME: Yashwant K. Malaiya

• My Research approach
  – Explore what has not been examined
  – Concepts contributed: Antirandom testing, Detectability Profile, New Vulnerability Discovery models, new Software reliability models

Areas in which I have published:

• Computer security
  – Vulnerability discovery
  – Risk evaluation
  – Assessing Impact of security breaches
  – Vulnerability markets

• Hardware and software
  – Testing & test effectiveness
  – Reliability and fault tolerance

• Results have been used by industry, researchers and educators
About me: Yashwant K. Malaiya

• Teaching
  – Computer Organization (CS270), Operating systems (CS370)
  – Computer Architecture (CS470)
  – Fault tolerant computing (CS530), Quantitative Security (CS559)

• Professional
  – Organized International Conferences on Microarchitecture, VLSI Design, Testing, Software Reliability
  – Computer Science Accreditation: national & international
  – Professional lectures
  – Advised more than 65 graduate students ..
ABOUT ME: Phil Sharp

• Education

• Experience
  – Instructor Computer Science Department Colorado State University
  – CS 110 Personal Computing, CS 270 Computer Organization
  – CS370 this semester
Contacting us

• Office hours, email addresses: Course website
  Yashwant Malaiya (CSB 356)
  Phil Sharp (CSB 248)
• Instructors: use Teams/email
  Yashwant Malaiya (CSB 356)
  Phil Sharp (CSB 248)
• TAs, Office Hours - MS Teams
  Richi Rodriguez, Graduate TA
  Mohit Kumar Katragadda, Graduate TA
  Xinyi Wang, Undergraduate TA
  Anteneh Zeleke, Undergraduate TA
• e-mail
  – The subject should start as CS370: ...
• Teams: lectures, discussions
• Canvas: Quizzes, assignments, tests, grades
Topics we will cover in CS 370

• Processes
  – Processes and Threads
  – CPU Scheduling
  – Process Synchronization and Deadlocks

• Memory Management
  – Address translation
  – Virtual memory

• File System interface and management
  – Storage Management
  – File systems

• Virtualization
  – Data centers
  – Containers
Textbook

• Operating Systems Concepts, 10th edition
  Avi Silberschatz, Peter Galvin, and Greg Gagne
  etext package

• May also use materials from other sources including
  – Andrew S Tanenbaum, Modern Operating Systems
  – Thomas Anderson and Michael Dahlin, Operating Systems Principles & Practice
  – System Documentation, articles, news etc.
On the schedule page

• Topics that will be covered and the order in which they will be covered
• Readings - chapters that I will cover
• May also see chapters mentions of other resources besides the textbook
• Schedule for when the assignments will be posted and when they are due
  – Subject to dynamic adjustment
Grading breakdown

• Assignments: 25%
  • Programming & written (note policies)

• Quizzes & interaction 20%
  – Weekend (Fri-Mon) and ICQ (Tu-Wed)

• Mid Term: 20%

• Project: 10%

• Final exam: 25%

• You can only take the midterm/final for your section. The three sections are graded independently.
Grading Policy I

- Letter grades will be based on the following standard breakpoints:
  - >= 90 is an A, >= 88 is an A-
  - >=86 is a B+, >=80 is a B, >=78 is a B-
  - >=76 is a C+, >=70 is a C,
  - >=60 is a D, and <60 is an F.

- We will not cut higher than this, but I may cut lower.

- There will be no make-up exams
  - Except for documented
    - required university event
    - acceptable family or medical emergency
Grading Policy II

• Plan: Every programming assignment will be posted 7-14 days before the due date. Written assignments will be posted 6-7 days before due date.
  – Every assignment will include specifications and will indicate it will be graded.

• Late submission penalty: 20% off for the 24 hours and a ZERO thereafter.

• Detailed submission instructions included in the assignment sheets (see canvas)

• Plan: Assignments will be graded within 2 weeks of submission

• The three sections are separately graded classes with the same standards
What will Quizzes and Tests include?

• We will only ask questions about what we teach, or ask you to study,
  – If I didn’t teach it, I won’t ask from that portion
  – Some on-line quiz questions about current state of technology may require you to search for an answer on the web
• If the concepts were covered in my lectures, slides or assignments
  – You should be able to answer the questions
  – You should be able to apply the concepts
• I will try to avoid questions about arcane aspects of some device controllers etc.
Exams & Assignments

• One mid-term
• The final exam is comprehensive, but more emphasis on the later part
• Quizzes: An on-line quiz every week Fri-Mon. ICQ interaction quizzes/feedback Tu-Wed.
• Programming (5-6) / written (1-2) assignments
• Occasional help-sessions Wednesday 5:30 PM Including coming week
  – Attend or view recordings (required)
• Self exercises: Do them yourselves
Term Project

• Group based
  – Second half of the semester

• Options:
  – Research paper on current/developing technology
    • Paper and presentation
    • Suggested topics will be announced
  – Development
    • IoT/Embedded system with sensor/communication
    • Design and evaluation needed
    • Demo and presentations
Electronic devices in lecture room

• Use of Laptops and other electronic devices are not permitted.

• Exception: Permitted only in the last row, with the pledge that you will
  – not distract others, turn off wireless
  – use it only for class related note taking, which must be submitted periodically

• Laptop use lowers student grades, experiment shows, Screens also distract laptop-free classmates

• The Case for Banning Laptops in the Classroom

• Laptop multitasking hinders classroom learning for both users and nearby peers
Be kind to everyone

• You will be courteous to fellow students, instructor and the teaching assistants
  – Classroom, outside, discussions on MS Teams

• Do not distract your peers
  – Turn microphones off unless needed
Help me help you

- Survey questions after each class (included in ICQ or Quizzes)
- You will provide a list of
  - 2 concepts you liked / followed clearly
  - 2 concepts you had problems with
- Questions of interest for the majority of the class will be addressed in the next class
Help Sessions

• Some Wednesdays 5:30 PM,

• TAs will discuss key techniques and skills
  – Participation strongly encouraged
  – Slides and videos will be on the web site
  – You must be familiar with Help Session materials

• Coming week
  – C pointers, dynamic memory allocation
  – Needed for upcoming programming assignment
EXPECTATIONS

• You are expected to attend all classes.
• You must be present during the complete class
• Assignments & quizzes must be done by yourself individually. We will check.
• Expect to work at least 6-8 hours per week outside of class
  – Designing, coding and testing programs
  – Reviewing material from class
  – Do research for the project
• Concentrate in the class. The class have many new terms and concepts.
Expert view on How to fail this class?

• Believing that you can learn via osmosis

• Missing lectures
  – “If you don’t have the discipline to show up, you will most likely not have the discipline to catch up”
  – Procrastinating

• Get started on the assignments late. Note that they incorporate new concepts, including multiple processes and threads.
Interactions on Teams

• You must join Team CompSci CS370 Spr21
• You can have discussions with the instructor, the GTA, and your peers
• But note
  – No code can be exchanged under any circumstances
  – No one takes over someone else’s keyboard
  – No code may be copied and pasted from anywhere, unless provided by us
• Appropriate use
From Operator to Operating System

Switchboard Operator

Computer Operators

©UCB
What is an Operating System?
Introductions

• We will finish that in 2-3 lectures

• When I call your name,
  
  – Please enable your camera, and speak
    
    • your name,
    
    • where you are from (city, country)
    
    • Degree you are working for, area of interest
What is an Operating System?

• Referee
  – Manage sharing of resources, Protection, Isolation
    • Resource allocation, isolation, communication
    • Isolation among threads, processes, users, virtual machines/containers

• Illusionist
  – Provide clean, easy to use abstractions of physical resources
    • Infinite memory, dedicated machine
    • Higher level objects: files, users, messages
    • Masking limitations, virtualization

Glue
  – Common services
    • Storage, Window system, Networking
    • Sharing, Authorization
    • Look and feel
A Modern processor: SandyBridge

- **Package:** LGA 1155
  - 1155 pins
  - 95W design envelope
- **Cache:**
  - L1: 32K Inst, 32K Data (3 clock access)
  - L2: 256K (8 clock access)
  - Shared L3: 3MB – 20MB
- **Transistor count:**
  - 504 Million (2 cores, 3MB L3)
  - 2.27 Billion (8 cores, 20MB L3)
Functionality comes with great complexity!

SandyBridge I/O Configuration

- Proc
- Caches
- Memory
- Busses
- I/O Devices:
  - Disks
  - Displays
  - Keyboards
- Controllers
- Networks
- adapters
- PCI Express* 2.0 Graphics
  - 16 lanes
  - 16 GB/s
- PCI Express* 2.0 Graphics
  - 8 lanes
  - 8 GB/s
- SandyBridge I/O Configuration
- Intel® Core™ processors
- DDR3 1333 MHz
- 14 Hi-Speed USB 2.0 Ports: Dual EHCI; USB Port Disable
- Intel® Integrated 10/100/1000 MAC
- PCIe® x1, SM Bus
- Intel® Gigabit LAN Connect
- Networks
- Intel® P67 Express Chipset
- Intel® ME Firmware and BIOS Support
- Intel® Rapid Storage Technology
- Intel® Extreme Tuning Support
- Intel® High Definition Audio
- 6 Serial ATA Ports: eSATA; Port Disable
- 8 PCI Express® 2.0
- DMI 20 Gb/s
- SPI 6 Gb/s
- up to 5 Gb/s each
- 480 Mb/s each
Short History of Operating Systems

• One application at a time
  – Had complete control of hardware

• Batch systems
  – Keep CPU busy by having a queue of jobs
  – OS would load next job while current one runs

• Multiple programs on computer at same time
  – Multiprogramming: run multiple programs at seemingly at the “same time”
  – Multiple programs by multiple or single user

• Multiple processors in the same computer

• Multiple OSs on the same computer
One Processor One program View

Early processors (LC-3 is an example)

• Instructions and data fetched from Main Memory using a program counter (PC)
• Traps and Subroutines
  – Obtaining address to branch to, and coming back
  – Using Stack Frames for holding
    • Prior PC, FP
    • Arguments and local variables
• Dynamic memory allocation and heap
• Global data
One Processor One program View

• External devices: disk, network, screen, keyboard etc.
• Device interface: Status and data registers
• User and Supervisor modes for processor
• I/O
  – Device drivers can use polling or interrupt
  – Interrupts need context switch
  – I/O done in supervisor mode
  – System calls invoke device drivers
What a simple view doesn’t include

- Cache between CPU and main memory
  - Makes the main memory appear much faster
- Direct memory access (DMA) between Main Memory and Disk (or network etc)
  - Transfer by blocks at a time
- Neglecting the fact that memory access slower than register access
- Letting program run concurrently (Multiprogramming) or with many threads
- Multiple processors in the system (like in Multicore)
- Multiple OSs in the same system
Information transfer in a system

- CPU Registers – (Caches) - Memory
  - CPU addresses memory locations
  - Bytes/words at a time
  - We will see some details

- Memory – (Controllers hw/sw) - external devices
  - Chunks of data
  - External devices have their own timing
    - DMA with interrupts
  - Disk is external!
I/O Hardware (Cont.)

- I/O Devices usually have registers where device driver places commands, addresses, and data
  - Data-in register, data-out register, status register, control register
  - Typically 1-4 bytes, or FIFO buffer
- Devices have addresses, used by
  - Direct I/O instructions
  - Memory-mapped I/O
    - Device data and command registers mapped to processor address space
I/O Transfer rates  MB/sec

- system bus
- HyperTransport (32-pair)
- PCI Express 2.0 (×32)
- Infiniband (QDR 12X)
- Serial ATA (SATA-300)
- Gigabit Ethernet
- SCSI bus
- FireWire
- hard disk
- modem
- mouse
- keyboard
Acknowledgments

• Past CS370 instructors, specifically Shrideep Pallickara for contributions to the class including materials and methods