

# Yashwant K. Malaiya

## 1 Education

Ph.D.	(Electrical Engineering)	Utah State University	1978
M.S.	(Electronics)	BITS, Pilani, India	1974
M.S.	(Physics)	Saugor University, India	1971
B.S.	(Physics, Math)	GD College, Damoh, MP, India	1969

## 2 Experience

1990-: Professor, Computer Science Dept.

1982-90: Associate Professor, Computer Science Dept., Colorado State University

1978-82: Assistant Professor, Dept. of Computer Science, State Univ. of New York at Binghamton

## 3 Chronology

1978: Erdős Number 2

1989: First Senior Member of IEEE in CS department

1995: Antirandom testing invented

1998: First patent in the CS department

2000: IEEE Third Millennium Medal

2005: Alhazmi-Malaiya Vulnerability Discovery Model

2018: h-index 36

## 4 Areas of research emphasis

Quantitative Security, Reliability, Fault modeling and testing, Testable and Fault-tolerant digital design

## 5 Professional Activities

### 5.1 Conferences

- General Chair, IEEE **International Symposium on Software Reliability Engineering (ISSRE)**, Denver, 2003.
- General Co-Chair, **IEEE Asian Test Symposium**, Shanghai, 1999.
- General Chair, **The Fourth International Symposium on Software Reliability Engineering (ISSRE)**, Denver, Nov. 1993.
- General Chair, **Sixth International Conference on VLSI Design (VLSI Design '93)**, Bombay, India, 1993.
- Program Chair, **Fifth International Conference on VLSI Design (VLSI Design '92)**, Bangalore, India, 1992.
- General Chair, **24th ACM/IEEE International Symposium on Microarchitecture (Micro-24)**, Albuquerque, 1991.
- General Chair, **IEEE International Workshop on IDDQ Testing (IDDQ-95)**, Washington D.C., October 1995, 2000.
- Chair Steering Committee, **IEEE International Workshop on IDDQ Testing**, 1996, 1997.
- Program Co-Chair, **The Eighth International Symposium on Software Reliability Engineering (ISSRE)**, Albuquerque, Nov. 1997.
- IEEE liaison for **International Conference on VLSI Design** 1994-1998.
- Finance chair, **IEEE International Symposium on Software Reliability Engineering (ISSRE)**, Pasadena, 2013.

### 5.2 Editing

- Guest editor, **IEEE Software**, Special issue on *Reliability Measurement*, July 1992, with P. Srimani.
- Guest Editor, **IEEE Design & Test**, Special issue on *VLSI Design*, Dec. 1992.
- Editor, *MicroArch*, Quarterly publication of IEEE CS TC on Microprogramming and Microarchitecture (1989-93)
- Digest of Papers - IEEE International Workshop on IDDQ Testing, Washington D.C., Oct. 1995.
- Editor-in-Chief, **Journal of Software Engineering and Applications**, 2011-cont.

### 5.3 Organizations

- Commissioner, **ABET Computing Accreditation Commission**, 2005
- Evaluator, **Computing Sciences Accreditation Board**, 1999-continuing.
- Member Editorial Board, ISRN Software Engineering 2011-cont., Intelligent Information management, 2011.
- PC member: ICQRMS 2011, ISSRE 1995-2014, ISSRE Program Board 2018.
- Vice chair, **IEEE CS Award Committee (1995-99)** (Service Awards).
- Vice Chair, **TCSE Software Reliability Engineering Committee** (1990-96).
- Chair, **Test Technology TC Subcommittee on Software Testing**, (1993-2002).
- Member, Executive Committee, **IEEE CS Technical Activities Board** (1988-98); **IEEE CS Conference and Tutorials Board** (1994, 2000, 2001);
- Chair, **IEEE-CS Technical Committee on Microprogramming and Microarchitecture**, (1988-92).
- Senior Member IEEE Computer Society.
- Founder, **India Association of Northern Colorado**, President: 1998-2000, 2012-13.

## 6 Reviewer

- **Journals** : IEEE Computer, IEEE Transactions on Dependable and Secure Computing, IEEE Trans. Computers, IEEE Trans. Reliability, IEEE Trans. Software Engineering, IEEE Software, IEEE Trans. CAD, IEEE Journal of Solid State Circuits, IEEE Trans. VLSI Systems, IEEE Design and Test, IEEE Trans on Systems, Man, and Cybernetics, Software Process: Improvement and Practice, Software Quality Journal, Empirical Software Engineering, Software Testing, Verification and Reliability, Journal of Digital Systems, Journal for Electronic Testing, Naval Research Logistics Quarterly, IEE Electronic Letters, IET Software, Int. Journal of Software Engineering, ISRN Software Engineering, Intelligent Information Management, Journal of Risk and Reliability, Computer Networks, Information Processing Letters, Information and Software Technology
- **Conferences** : Int. Symp. on Software Reliability Engineering, International Symposium on Fault-tolerant Computing, International Test Conference, Design Automation Conference, IEEE Tencon, Int. Symp. and Work. on Microprogramming and Microarchitecture, Asian Test Symposium, VLSI Design, IEEE/IFIP Int Conference on Embedded & Ubiquitous Computing Reliability Engineering & System Safety, IEEE Int. Conf. on Computer Science and Information Technology etc.
- **Funding Agencies** : National Research Council, NSF, Research Grants Council, Hong Kong, Uberoi foundation.
- **Publishers** : Computer Science Press, West Educational Publishing, John Wiley, McGraw-Hill, Asken, Columbia University Press, Cambridge University Press.
- **External Reviewer for Universities** : Roorkee University, State University of New York, Georgia Tech, University of Wyoming, Florida Atlantic University, Chinese University of Hong Kong, West Virginia State, University of Jordan, Thapar University.

## 7 Courses

Graduate: Fault-Tolerant Computing, Testable Systems, Advanced Fault-Tolerant Computing

Undergraduate: Operating systems, Logic Design, Computer Organization and Assembly Language, Computer Architecture, Interactive Programming with Java, Microprogramming and bit-sliced devices, Microcomputer programming and interfacing, Discrete structures, Data Communications

## 8 Recognitions

- Invited tutorial, Embedded Software Testing, IEEE VLSI Test Symposium, Las Vegas, 2017.
- Visiting Professor, Graduate School of Engineering, Hiroshima University, Summer 2016.
- Invited lecture, Reliability Allocation for Software projects using Static/Dynamic Software Reliability Modeling, OSRJ, TMU, Tokyo, August 2016.
- Keynote, 2014 International Conf. on Knowledge and Software Eng., “Security Vulnerabilities: Risks from Discovery to Exploitation”
- IEEE CS Certificate of Appreciation, 2003, “for exceptional effort as General Chair in organizing and running a successful ISSRE 2003”.
- IEEE CS Meritorious Service Award, 2002 “For providing skilled management and guidance to the IEEE International Workshop on Defect Based Testing for over five years”.
- IEEE Third Millennium Medal, 2000.
- Best Paper Award, ISSRE 1997 (see Publications).
- IEEE CS Golden Core Award, June 1996.
- IEEE CS Certificate of Appreciation Award, Oct. 20, 1996 "*For significant leadership contribution to the International IDDQ Test Workshop as Chairman, 1995*"

- IEEE CS Meritorious Service Award, Feb. 1993. *For Technical and administrative leadership while serving as Chair of the Technical Committee on Microprogramming and Microarchitecture*
- Honorary appointment as Professor, Electrical Eng. Dept., CSU.
- Invited lectures at China Academy of Sciences, Beijing, and Shanghai University of Science and Technology (3 weeks), 1989.
- Merit List, University of Saugor, 1971.
- Rotary Club Award: Top B.Sc. student, GD College, Damoh, 1969.
- Sanskrit Scholarship, GMHS School, Damoh, 1963-66.
- Named in *American Men and Women of Science*.

## Publications

### 1 Books/Chapters:

1. Y. K. Malaiya, "Software Reliability: A Quantitative Approach," in **System Reliability Management: Solutions & Technologies**, Ed. Adarsh Anand, CRC Press 2018, pp. 221-252
2. S. C. Jain and Y. K. Malaiya, "Jain Population Predicament: Need to Learn from the Parsi and Jewish Situations," in **Studies in Jain Demography, 1881-2011**, Ed. P. C. Jain, Rawat Publications 2018, p. 165-172.
3. Y. K. Malaiya, "Interactions among the Dharmic Traditions," in **Compassion in the 4 Dharmic Traditions**, Editor: Ved P. Nanda, Prabhat Prakashan, Delhi, 2016, pp 70-88.
4. Y. K. Malaiya, "Optimal Reliability Allocation," **Wiley Encyclopedia of Operations research and Management Science**, John Wiley & Sons, Jan. 2011.
5. Y.K. Malaiya, "Software Reliability Management," **Encyclopedia of Library and Information Sciences**, Taylor and Francis, Editor: S. Lee, Third Edition, 1: 1, 4901 — 4912, February 2010.
6. Y. K. Malaiya, "Reliability Allocation," **Encyclopedia of Statistics in Quality and Reliability**, John Wiley & Sons, March 2008, 5 pages.
7. Y. K. Malaiya, "Software Reliability and Security," in **Encyclopedia of Library and Information Science**, 2005. Y.K. Malaiya,
8. "Software Reliability", **Encyclopedia of Library and Information Science**, Editors: A. Kent and C.M. Hall, Pub. Marcel Dekker, Inc. 2003, pp. 2688 - 2698.
9. Y.K. Malaiya, "Software Reliability", **Encyclopedia of Library and Information Science**, Editors: A. Kent and C.M. Hall, Pub. Marcel Dekker, Inc. V. 67, May 2000, pp. 341-357.
10. Y.K. Malaiya, "Automated Test Software", for **Wiley Encyclopedia of Electrical and Electronics Engineering**, Editor: J.G. Webster, Pub. John Wiley & Sons, Inc. 1999, pp. 135-141.
11. Karunanithi and Y.K. Malaiya, "Neural Networks for Software Reliability", Chapter in **Handbook on Software Reliability Engineering**, Ed. M. Lyu, Publisher: McGraw-Hill, 1996. 108. 1
12. Y.K. Malaiya, "Golapurva Anvaya: Eksa Parichaya" (Hindi), in **Golapurva Jain Samaj: Itihas evam Sarvekshana** ed. Dr. Surendra K. Jain, Pub. Paras Research Inst., Sagar, 1996, pp. 32-44.
13. C.C. Liaw, S.Y.H. Su and Y.K. Malaiya, "Test Generation for Delay Faults using Stuck-at Fault Test Set," **25<sup>th</sup> Anniversary Compendium of papers**, International Test Conference, 1994, pp. 206-214 (selected for republication).
14. **Bridging Faults and IDDQ Testing**, Editors: Y.K. Malaiya and R. Rajsuman, *IEEE Computer Society Press Technology Series*, 1992.
15. **Software Reliability Models: Theoretical Development, Evaluation and Applications**, Editors: Y.K. Malaiya and P. Srimani, *IEEE Computer Society Press Technology Series*, 1990.
16. Y.K. Malaiya, "Identification of Golladesh and Gollacharya on the basis of Kuvalayamala-kaha," in **Jaganmohanlal Shastri Felicitation Volume**, JML Sadhuvad Samiti, 1990 (in Hindi) pp. 448-454.
17. Y.K. Malaiya, "On the Golapurva Caste" in **Vyakaranacharya Banshidhar Felicitation Volume**, 1990 (in Hindi), pp. 103-130.
18. C.C. Liaw, S.Y.H. Su and Y.K. Malaiya, "Test Generation for Delay Faults using Stuck-at Fault Test Set," **VLSI Support Technologies: Computer-Aided Design, Testing and Packaging**, Ed. Rex Rice, IEEE Computer Society Press, 1982, pp. 281-290 (selected for republication).

### 2 Patents

1. W.K. AlAssadi, A.P. Jayasumana and Y.K. Malaiya, "IDDQ Testing of Integrated Circuits" Patent granted May 26, 1998.

### 3 Software Tools

1. **ROBUST**, *An integrated Software Reliability tool*. MS Windows, X-Windows, <http://www.cs.colostate.edu/testing/robust/>.

## 4 Journals

- 1 P. Xiao, Y. Yin, B. Liu, B. Jiang, Y. K. Malaiya, "Adaptive Testing Based on Moment Estimation", *IEEE Trans. on Systems, Man, and Cybernetics: Systems*, Dec 2017, pp. 1-12.
- 2 L. Liu, Y. Yin, Z. Zhang, Y.K. Malaiya, "Redundant Design in Interdependent Networks", *PLOS ONE* Vol. 11, October 20, 2016.
- 3 H. Joh and Y.K. Malaiya, "Periodicity in Software Vulnerability Discovery, Patching and Exploitation", *International Journal of Information Security*, Nov 2017, pp pp 673–690.
- 4 A. A. Younis, Y. K. Malaiya, and I. Ray, "Assessing Vulnerability Exploitability Risk Using Software Proprieties", *Software Quality Journal*, March 2016, Volume 24, Issue 1, pp. 159-202.
- 5 A. M. Algarni, Y. K. Malaiya, "Software Vulnerability Markets: Discoverers and Buyers," *Int. Journal of Computer, Information Science and Engineering*, Vol:8 No:3, 2014, pp. 71-81.
- 6 H. Joh, Y. K. Malaiya, "Modeling Skewness in Vulnerability Discovery", *Quality and Reliability Engineering International*, Vol. 30, Issue 8, pp. 1445–1459, Dec. 2014.
- 7 Y.K. Malaiya, "Jain Renaissance of Fifteenth Century", *Jain Prachin Tirth Jirnoddhar*, Year 10, Number 8, p. 24-26, July 2013.
- 8 S.-W. Woo, H. Joh, O. H. Alhazmi and Y. K. Malaiya, "Modeling Vulnerability Discovery Process in Apache and IIS HTTP Servers", *Computers & Security*, Vol. 30, Issue 1, 2011, pp. 50-62.
- 9 S.H. Wu, S. Jandhyala, Y. K. Malaiya, A. P. Jayasumana, "Antirandom Testing: A Distance Based Approach," *VLSI Design*, 2008, 9 pages, 2008. doi:10.1155/2008/165709.
- 10 O. H. Alhazmi and Y. K. Malaiya, "Application of Vulnerability Discovery Models to Major Operating Systems," *IEEE Trans. Reliability*, March 2008, pp. 14-22.
- 11 Y. K. Malaiya, "Giants from the Annals of Jain History", *Jinamanjari*, 37.1, 2008, 3-29.
- 12 O. H. Alhazmi, Y. K. Malaiya , I. Ray, " Measuring, Analyzing and Predicting Security Vulnerabilities in Software Systems," *Computers and Security Journal*, Volume 26, Issue 3, May 2007, Pages 219-228.
- 13 Y.K. Malaiya, N. Li, J. Bieman, R. Karcich, "Software Test Coverage and Reliability," *IEEE Trans. Reliability*, Dec. 2002, pp. 420-426.
- 14 Y.K. Malaiya, "Kundalpur's Past Three Centuries," *Arhat Vacan*, Vol. 13, no. 3-4, 2001 pp. 5-13.
- 15 S.M. Menon, Y.K. Malaiya, A.P. Jayasumana and C.Q Tong, "Operational and Test Performance in the Presence of Built-in Current Sensors," *Int. Journal of VLSI Design*, 1997, V. 5, No. 3, pp. 285-298.
- 16 S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "ECL Storage Elements: Modeling of Faulty Behavior," *IEEE Trans. Circuits & Systems-II*, Nov. 1997, pp. 970-974.
- 17 M. Menon, A. P. Jayasumana and Y. K. Malaiya, "BiCMOS Domino: A Novel High-Speed Dynamic BiCMOS Logic," *Int. Journal of Electronics*, 1997, V. 83, No. 2, pp. 177-189.
- 18 S.M. Menon, A.P. Jayasumana and Y.K. Malaiya "Testable Design for BiCMOS Stuck-Open Fault Detection using Single Patterns" *IEEE Journal of Solid State Circuits*, Aug. 1995, pp. 855-863.
- 19 S.M. Menon, A.P. Jayasumana and Y.K. Malaiya, "Manifestation of Faults in Single and Double BJT BiCMOS Logic Gates," *Proc. IEE, Pt. E, Computers and Digital Techniques*, Vol. 142, No. 2, pp. 135-144, March 1995.
- 20 Y.K. Malaiya, A.P. Jayasumana, Q. Tong and S. Menon, "Resolution Enhancement in IDDQ testing for Large ICs" *International Journal of VLSI Design*, Vol. 1, No. 4, pp. 277-284.
- 21 N. Karunanithi, D. Whitley and Y.K. Malaiya, "Prediction of Software Reliability using a Connectionist Approach," *IEEE Trans. Software Engineering*, Sept. 1992, pp. 563-574.
- 22 Y.K. Malaiya, "Golshivai and Golladeshadhipa" *Arhat-Vachan*, 1994 (in Hindi).
- 23 W.K. Al-Assadi, D. Lu, A.P. Jayasumana, Y.K. Malaiya and C.Q. Tong, "Data Feed-through Faults in circuits using Unlocked Storage Elements," *Electronic Letters*, Vol. 30, No. 10, May 12, 1994, pp. 764-765.
- 24 Y.K. Malaiya, A. von Mayrhauser and P. Srimani, "An Examination of Fault Exposure Ratio," *IEEE Trans. Software Engineering*, Nov. 1993, pp. 1087-1094.
- 25 S.M. Menon, A.P. Jayasumana, Y.K. Malaiya and D.R. Clinkinbeard, "Modeling and Analysis of Bridging Faults in Emitter-Coupled Logic (ECL) Circuits," *IEE Proceedings, Computer and Digital Techniques*, Vol. 140, No. 4, July 1993, pp. 220-226.
- 26 W. Alassadi, Y.K. Malaiya and A.P. Jayasumana, "Faulty Behavior of Storage Elements and its Effects on Sequential Circuits" *IEEE Trans. VLSI Systems*, Dec. 1993 pp. 446-452.
- 27 Y.K. Malaiya, "The Sravakas of Madanasagarapura in the Chandel Period" *Anekanta*, July-Sept. 1993 (in Hindi).
- 28 Y.K. Malaiya, N. Karunanithi and P. Verma, "Predictability of Software Reliability Models," *IEEE Trans. Reliability*, Dec. 1992, pp. 539-546.
- 29 N. Karunanithi, D. Whitley and Y.K. Malaiya, "Applying Neural Networks to Software Reliability Prediction," *IEEE Software*, July 1992, pp. 53-59.
- 30 Y. Min, Y.K. Malaiya and B. Jin, "Analysis of Detection Capability of Parallel Signature Analyzers," *IEEE Trans. Computers*, Vol. 40, No. 9, Sept. 1991, pp. 1075-1081.
- 31 A.P. Jayasumana and Y.K. Malaiya and R. Rajsuman, "Design of CMOS Circuits for Stuck-Open Fault Testability," *IEEE Journal of Solid State Circuits*, Vol. 26, No.1, January 1991, pp. 58-61.

- 32 A.P. Jayasumana, W. Al-assadi and Y.K. Malaiya, "On Pass Transistor Logic Design," *International Journal of Electronics*, Vol. 70, No. 4, April 1991, pp. 739-749.
- 33 S. Feng and Y.K. Malaiya, "Optimization of Test Parallelism with Limited Hardware Overhead," *Microelectronics and Reliability*, Vol. 31, No. 2, 1991, pp. 271-276.
- 34 Y.K. Malaiya, "The Sravakas of Golladesh and Gollapura," *Anekanta*, Vol. 44, No. 1, Jan. 1991, pp. 4-8 (in Hindi).
- 35 Y. Min, Y.K. Malaiya and B. Jin, "Aliasing errors in parallel signature analyzers," *Journal of Computer Science and Technology*, V. 5, No. 1, January 1990, pp. 25-40.
- 36 S.M. Menon, A.P. Jayasumana and Y.K. Malaiya, "Fault Modeling for ECL Devices," *Electronic Letters*, Vol. 26, NO. 15, July 19, 1990, pp. 1105-1108
- 37 R. Rajsuman, Y.K. Malaiya and A.P. Jayasumana, "Reprogrammable FPLA with Universal Test Set," *Proc. IEE*, Vol. 137, Pt. E, No. 6, Nov. 1990, pp 437-441.
- 38 R. Rajsuman, Y.K. Malaiya and A.P. Jayasumana, "Limitations of Switch Level Analysis for Bridging Faults," *IEEE Trans. CAD.*, Vol. 8, No. 7, July 1989, pp. 807-811.
- 39 R. Rajsuman, A.P. Jayasumana and Y.K. Malaiya, "CMOS Stuck-open Fault Detection in Presence of Glitches and Timing Skews," *IEEE Journal of Solid State Circuits*, Vol. 24, No. 4, August 1989, pp. 1055-1061.
- 40 R. Rajsuman, Y.K. Malaiya and A.P. Jayasumana, "CMOS Stuck-open Fault Testability," *IEEE Journal of Solid State Circuits*, Vol. 24, No. 1, pp. 193-194, Feb. 1989.
- 41 Y. Min, Y.K. Malaiya and B. Gupta, "On the Computational Complexity of Test Generation for ETG PLAs," *IEE Proceedings* Vol. 136, Pt. E, No. 2, March 1989, pp. 107-111.
- 42 R. Rajsuman, A.P. Jayasumana and Y.K. Malaiya, "On Testing of Complex Gates," *Electronic Letters*, Vol. 23, No. 16, July 30, 1987, pp. 813-814.
- 43 Y.K. Malaiya, "Analyzing Data for CMOS Leakage Faults," *Microelectronics and Reliability*, Vol. 25, No. 5, 1985, pp. 943-948.
- 44 Y.K. Malaiya and R. Narayanaswamy, "Modeling and Testing for Timing Faults in Synchronous Sequential Circuits," *IEEE Design and Test of Computers*, Vol. 1, No. 4, November 1984, pp. 62-74.
- 45 Y.K. Malaiya and S.Y.H. Su, "Analysis of an Important Class of Non-Markov Systems," *IEEE Trans. Reliability*, Vol. R-31, No. 1, April 1982, pp. 64-68.
- 46 Y.K. Malaiya, "Linearly Correlated Intermittent Failures," *IEEE Trans. Reliability*, Vol. 31, No. 2, June 1982, pp. 211-215.
- 47 Y.K. Malaiya and S.Y.H. Su, "Reliability Evaluation for Hardware Redundancy Fault-Tolerant Systems with Intermittent Faults," *IEEE Trans. Computers*, Vol. C-30, No. 8, August 1981, pp. 600-604.
- 48 C.C. Liaw, S.Y.H. Su and Y.K. Malaiya, "Test-Experiments for Detection and Location of Intermittent Faults in Sequential Circuits," *IEEE Trans. Computers*, Vol. C-30, No. 12, December 1981, pp. 989-995.
- 49 S.Y.H. Su, I. Koren, Y.K. Malaiya, "A Continuous Parameter Markov Model and Detection Procedures for Intermittent Faults," *IEEE Trans. Computers*, Vol. C-27, No. 6, June 1978, pp. 567-570.
- 50 Y.K. Malaiya, "An Examination of the Sixteenth Chapter of Vardhamana Purana," *Anekanta*, Vol. 27, No. 2, August 1974, pp. 58-64 (in Hindi).
- 51 Y.K. Malaiya, "On the Golapurvas," *Anekanta*, Vol. 25, No. 2, May 1972, pp. 68-72 (in Hindi).
- 52 Y.K. Malaiya, "Research Notes," *Anekanta*, Vol. 24, No. 5, November 1971, pp. 213-214 (in Hindi).

## 5 Conferences

1. R. Abdunabi and Y.K. Malaiya, "The Impact of Test Case Prioritization on Test Coverage versus Defects Found", Proc. 2017 Int. Conf. on Software Eng. Research and Practice, pp. 10-15.
2. O.H. Alhazmi and Y.K. Malaiya, "A Survey of Disaster Recovery Tiers Schemes", Proc. 31st Int. Conf. on Comp. and Their Applications (CATA), 2016, pp. 201-206.
3. A. M. Algarni and Y.K. Malaiya, "A Consolidated Approach for Estimation of Data Security Breach Costs", 2nd Int. Conf. on Information Management (ICIM), London, 2016, pp. 26-39.
4. A. Younis, Y. Malaiya and I. Ray, "Evaluating CVSS Base Score Using Vulnerability Rewards Programs", Proc. 31th Int. Information Security and Privacy Conference, IFIP SEC, Ghent, Belgium, 2016, pp. 62-75.
5. A. Younis, Y. Malaiya, C. Anderson and I. Ray "To Fear or Not to Fear That is the Question: Code Characteristics of a Vulnerable Function with an Existing Exploit", ACM Conference on Data and Application Security and Privacy 2016, pp. 97-104.
6. A. Younis and Y.K. Malaiya, "Comparing and Evaluating CVSS Base Metrics and Microsoft Rating System", The 2015 IEEE Int. Conf. on Software Quality, Reliability and Security, pp. 252-261.
7. A. A. Younis, Y. K. Malaiya, and I. Ray, "Using Attack Surface Entry Points and Reachability Analysis to Assess the Risk of Software Vulnerability Exploitability", Proc. 2014 IEEE 15th International Symposium on High-Assurance Systems Engineering (HASE 2014), Miami, January, 2014, pp. 1-8.
8. O.H. Alhazmi and Y.K. Malaiya, "Are the Classical Disaster Recovery Tiers Still Applicable Today?", Proc. Int. Symp. Software Reliability Eng. Workshops, (ISSREW), pp. 114-115, Nov. 2014.

9. A. Younis, Y.K. Malaiya, "Using Software Structure to Predict Vulnerability Exploitation Potential," Int. Conf. on Software Security and Reliability-Companion (SERE-C), pp.13-18, June 30-July 2 2014.
10. Y. K. Malaiya, "Interactions among Dharmic Traditions: with emphasis on Jainism, Buddhism and Hinduism," Uberoi Foundation Experts Meeting, Naropa University, Boulder, Sept 13, 2014.
11. A. M. Algarni, and Y. K. Malaiya, "Most Successful Vulnerability Discoverers: Motivation and Methods", Int. Conference on Security and Management (SAM 2013), Las Vegas, July 2013, pp. 3-9.
12. O. H. Alhazmi and Y.K. Malaiya, "Evaluating Disaster Recovery Plans Using the Cloud", Proc. Reliability and Maintainability Symposium (RAMS 2013), Orlando, January 2013, pp. 37-42.
13. A. A. Younis and Y. K. Malaiya, "Relationship between Attack Surface and Vulnerability Density: A Case Study on Apache HTTP Server", ICOMP'12, 2012 Int. Conference on Internet Computing, July 2012, pp. 197-203.
14. O. H. Alhazmi and Y.K. Malaiya, "Assessing Disaster Recovery Alternatives: On-site, Colocation or Cloud", Proc. 23rd IEEE Int. Symposium on Software Reliability Engineering Workshop, 2012, pp. 19-20.
15. H. Joh and Y. K. Malaiya, "Defining and Assessing Quantitative Security Risk Measures Using Vulnerability Lifecycle and CVSS Metrics," Proc. Int. Conference on Security and Management (SAM11), 2011, pp.10-16.
16. A. A. Younis, H. Joh, and Y. K. Malaiya, "Modeling Learningless Vulnerability Discovery using a Folded Distribution," Proc. Int. Conference on Security and Management (SAM11), 2011.
17. HyunChul Joh and Yashwant K. Malaiya, "A Framework for Software Security Risk Evaluation using the Vulnerability Lifecycle and CVSS Metrics" International Workshop on Risk and Trust in Extended Enterprises (RTEE'2010), November 2010, pp. 430-434.
18. X. He, Y. K. Malaiya, A. P. Jayasumana, K. P. Parker and S. Hird, "Principal Component Analysis-Based Compensation for Measurement Errors Due to Mechanical Misalignments in PCB Testing" Proc. 41st International Test Conference (ITC'10), Austin, Texas, November 2010, pp.16.1.1-10.
19. H. Joh and Y. K. Malaiya, "Modeling Skewness in Data with S-shaped Vulnerability Discovery Models" Proc. Int. Symp. Software Reliability Eng. (ISSRE), Fast Abstracts, November 2010, pp. 406-407.
20. H. Joh, S. Chaichana and Y. K. Malaiya, "Short-term Periodicity in Security Vulnerability Activity" Proc. Int. Symp. Software Reliability Eng. (ISSRE), Fast Abstracts, November 2010, pp. 408-409.
21. A. P. Jayasumana, Y. K. Malaiya, X. He, K. P. Parker and S. Hird, "Compensation for measurement errors due to mechanical misalignment in PCB testing," IEEE 9th International Board Test Workshop (BTW'10), Fort Collins, CO, Sept. 14 - 16, 2010.
22. X. He, Y. K. Malaiya, A. P. Jayasumana, K. P. Parker and S. Hird, "An Outlier Detection Based Approach for PCB Testing," Proc. IEEE Int. Test Conference, Nov. 2009, pp. 1-10.
23. X. He, Y. Malaiya, A. P. Jayasumana, K. P. Parker and S. Hird, "Outlier Detection in Capacitive Open Test Data Using Principal Component Analysis," Presented at the IEEE 8th International Board Test Workshop (BTW'09), Fort Collins, CO, Sept. 2009.
24. H. Joh and Y. K. Malaiya, "Seasonal Variation in the Vulnerability Discovery Process, " Proc. 2nd IEEE Int. Conf. Software Testing, Verification, and Validation, April 2009, pp. 191-200.
25. H. Joh and Y. K. Malaiya, "Seasonality in Vulnerability Discovery in Major Operating Systems and Web Applications," Fast Abstract, Proc. Int. Symp. Software Reliability Eng., Nov. 2008, pp. 297-298.
26. H. Joh, J. Kim and Y. K. Malaiya, "Vulnerability Discovery Modeling using Weibull Distribution," Fast Abstract, Proc. Int. Symp. Software Reliability Eng., Nov. 2008, pp. 299-300.
27. J. Kim, Y. K. Malaiya and I. Ray, "Vulnerability Discovery in Multi-Version Software Systems," Proc. 10th IEEE Int. Symp. on High Assurance System Engineering (HASE), Dallas, Nov. 2007, pp. 141-148.
28. A. Sanyal, A. Sokolov, Y. Malaiya and D. Whitley, " A Co-evolutionary Algorithm for Dynamic Power Minimization During Scan Testing," 16th IEEE North Atlantic Test Workshop, May 2007, pp. 13-18.
29. Jinyoo Kim, Omar Alhazmi and Yashwant Malaiya, "Vulnerabilities in Browsers: Trends in Internet Explorer and Firefox", Supp. Proc. ISSRE Fast Abstracts, Nov. 2006, pp 1-2.
30. S-W. Woo, O.H. Alhazmi and Y.K. Malaiya, "An Analysis of the Vulnerability Discovery Process in Web Browsers", Proc. 10th IASTED Int. Conf. on Software Engineering and Applications, Nov. 2006.
31. O.H. Alhazmi and Y.K. Malaiya, "Measuring and Enhancing Prediction Capabilities of Vulnerabilities Discovery Models for Apache and IIS HTTP Servers ", Proc. Int. Symp. Software Reliability Eng, Nov. 2006, pp. 343-352.
32. O.H. Alhazmi, S-W. Woo, and Y.K. Malaiya, "Security Vulnerability Categories in Major Software Systems", Proc. IASTED Int. Conference on Communication, Network and Information Security, Oct. 2006. pp.138-143.
33. S-W. Woo, O.H. Alhazmi and Y.K. Malaiya, "Assessing Vulnerabilities in Apache and IIS HTTP Servers", Proc. IEEE Int. Symp. on Dependable, Autonomic and Secure Computing (DASC'06), Sept.-Oct. 2006, pp. 103-110.
34. A. Sharma, A. P. Jayasumana and Y.K. Malaiya, "X-IDDQ: A Novel Defect Detection Technique using IDDQ Data," Proc. IEEE VLSI Test Symposium, April-May 2006, pp. 180-185.
35. O. H. Alhazmi and Y. K. Malaiya, "Prediction Capabilities of Vulnerability Discovery Models," Proc. Reliability and Maintainability Symposium, Jan 2006, pp.86-91.
36. O. H. Alhazmi and Y. K. Malaiya, "Modeling the Vulnerability Discovery Process," Proc. Int. Symp. Software Reliability Eng, Nov. 2005, pp. 129-138.
37. Y. K. Malaiya, C. Braganza and C. Sutaria, "Early Applicability of the Coverage/Defect Model," Supp. Proc. Int. Symp. Software Reliability Eng, Nov. 2005, pp. 4.27-4.28.
38. A. Sokolov, A. Sanyal, D. Whitley, Y.K. Malaiya, "Dynamic Power Minimization During Combinational Circuit Testing as a

- Traveling Salesman Problem,” Proc. 2005 IEEE Congress on Evolutionary Computation, Sept. 2005, pp. 1088-1095.
39. O. H. Alhazmi, Y. K. Malaiya and I. Ray, "Security Vulnerabilities in Software Systems: A Quantitative Perspective," Proc. IFIP WG 11.3 Working Conference on Data and Applications Security, August 2005, pp. 281-294.
  40. A. S. Banthia, A. P. Jayasumana and Y. K. Malaiya, "Data Size Reduction for Clustering Based Binning of ICs Using Principal Component Analysis (PCA)", Proc. IEEE Int. Workshop on Defect Based Testing, May 2005., pp. 27-33.
  41. O. Alhazmi, Y.K. Malaiya, "Quantitative Vulnerability Assessment of System Software," Proc. IEEE Reliability and Maintainability Symposium, Jan. 2005, pp. 615-620.
  42. J. Chen and Y.K. Malaiya, "Augmenting Test Case Generation using Statechart," Proc. Int. Conf. Software Eng. Research and Practice, June 2004, pp. 608-614.
  43. D. Henry and Y.K. Malaiya, "A Visualization System for Sliding Windows Protocol," Proc. ACM/IEEE Frontiers in Education Conference, Nov. 2003, pp. T2C1-T2C6.
  44. R.P. Turakhia, A.P. Jayasumana and Y.K. Malaiya, "Clustering based Production Line binning of ICs based on IDDQ," Proc. Int. Work. on Defect Based Testing, April 2003, pp. 65-73.
  45. H.V. Kantamneni, S.R.Pillai and Y.K. Malaiya "Structurally Guided Testing," in Supp. Proc. Int. Symp. Software Reliability Eng., Nov 2002, pp. 137-138.
  46. R.Ye and Y.K. Malaiya, "Relationship between test effectiveness and Coverage," in Supp. Proc. Int. Symp. Software Reliability Eng., Nov 2002, pp. 159-160.
  47. Rao, A.P. Jayasumana and Y.K. Malaiya "Optimal Clustering and Statistical Identification of Defective ICs using IDDQ Testing," Proc. IEEE Int Work. on Defect Based Testing, April 2000, pp. 30-35.
  48. Y. K. Malaiya and J. Denton "Module Size Distribution and Defect Density," Proc. IEEE International Symposium on Software Reliability Engineering, Oct. 2000, pp. 62-71.
  49. Y. K. Malaiya and J. Denton "Requirement Volatility and Defect Density," Proc. IEEE Int. Symp. Software Reliability Engineering, Nov. 1999, pp. 285-294.
  50. Palaniswamy, A. Jayasumana Y. K. Malaiya "A Neural Network based Approach for Testing Analog Circuits with Frequency Domain Classification and Time Domain Testing", Int. Work. on System Test Diagnosis, 1999.
  51. S.H. Wu, Y.K. Malaiya and A.P. Jayasumana, "Antirandom vs. Pseudorandom Testing" Proc. IEEE International Conference on Computer Design, Oct. 1998.
  52. M.N. Li, Y.K. Malaiya and J. Denton, "Estimating the Number Defects: A Simple and Intuitive Approach" Proc. IEEE International Symposium on Software Reliability Engineering, Industrial Practices, November 1998, pp. 307-315.
  53. Y.K. Malaiya and J. Denton, "Estimating the Number of Residual Defects" Proc. IEEE High Assurance Systems Engineering Symposium (HASE '98), November 1998, pp. 98-105.
  54. Y. K. Malaiya and J. Denton, "What Do the Software Reliability Growth Model Parameters Represent?" Int. Symp. on Software Reliability Engineering, 1997. pp. 124-135.
  55. H. Yin, Z. Lebne-Dengel and Y. K. Malaiya, "Automatic Test Generation using Checkpoint Encoding and Antirandom Testing" Int. Symp. on Software Reliability Engineering, 1997, pp. 84-95. Best Paper Award.
  56. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "Input Pattern Classification for Detection of Stuck-on and Bridging Faults Using IDDQ Testing in BiCMOS and CMOS Circuits," Proc. International Conference on VLSI Design, Jan.1997, pp. 545-546.
  57. S. M. Menon, A. P. Jayasumana and Y. K. Malaiya, "Input pattern classification for transistor level testing of bridging faults in BiCMOS circuits," Proc. IEEE 6th Great Lakes Symposium on VLSI, March 1996, pp. 214-219.
  58. N. Li and Y.K. Malaiya, "Fault Exposure Ratio: Estimation and Applications" Proc. IEEE Int. Symp. Software Reliability Engineering, 1996, pp. 372-381.
  59. R.V. Vogety, A.P. Jayasumana and Y.K. Malaiya, "Interconnection of FDDI-II Networks Through an ATM Backbone, An Analysis," Proc. 20th Conf. on Local Computer Networks, pp. 150-157, Oct. 1995.
  60. S. M. Menon, A. P. Jayasumana and Y. K. Malaiya, "A Novel High-Speed BiCMOS Domino Logic Family," Proc. of the 1995 IEEE Intl. Symp. on Circuits and Systems (ISCAS), pp. 21-24, May 1995.
  61. W.K. Al-Assadi, A.P. Jayasumana, Y.K. Malaiya, "A Bipartite Differential IDDQ Testable Static RAM Design" Proc. Int. Workshop on Memory Tech. Design and Testing, pp. 36-41, August 1995.
  62. W.K. Al-Assadi, Y.K. Malaiya and A.P. Jayasumana,, "Differential IDDQ Testable Static RAM Architecture" Proc. IEEE Int. Work. on IDDQ Testing, pp. 54-59, Oct. 1995.
  63. Yashwant K. Malaiya "Antirandom Testing: Getting the Most out of Black Box Testing" Proc. IEEE Int. Symp. on Software Reliability Engineering, pp. 86-95, Oct. 1995.
  64. N. Li and Y.K. Malaiya "ROBUST: A Next Generation Software Reliability Engineering Tool" Proc. IEEE Int. Symp. on Software Reliability Engineering, pp. 375-380, Oct. 1995.
  65. W.K. Al-Assadi, A.P. Jayasumana, Y.K. Malaiya, "On Fault Modeling and Testing of Content Addressable Memories," Proc. Int. Memory Tech. Design and Test Workshop, Aug. 1994. pp. 78-83.
  66. N. Li and Y.K. Malaiya, "On Input Profile Selection for Software Testing," Proc. Int. Symp. Software Reliability Engineering, Nov. 1994, pp. 196-205.
  67. Y.K. Malaiya, N. Li, J. Bieman, R. Karcich and B. Skibbe, "The Relationship between Test Coverage and Reliability" Proc. Int. Symp. Software Reliability Engineering, Nov. 1994, pp.186-195.
  68. Y.K. Malaiya and N. Li, "Software Reliability Modelling Approaches: Current Status," Proc. Int. Symp. Young Investigators on Information/Computer/Control, Beijing, Jan. 1994.

69. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, C.Q. Tong, "The Effect of Built-in Current Sensors (BICS) on Operational and Test Performance," *Proc. VLSI Design*, Jan. 1994, pp.187-190.
70. S.M. Menon, A.P. Jayasumana and Y.K. Malaiya, "Input pattern Classification for Transistor Level Testing of BiCMOS Circuits" *Proc. IEEE VLSI Test Symposium*, 1994, pp. 457-462.
71. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "Testable Design of BiCMOS Circuits for Stuck-Open Fault Detection using Single Patterns" *VLSI Test Symposium*, April 1993, pp. 296-302.
72. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "Bridging Faults in BiCMOS Circuits," *Proc. 5th NASA Symp. on VLSI Design*, Nov. 1993, pp. 7.1.1-7.1.10.
73. S.M. Menon, A.P. Jayasumana and Y.K. Malaiya "Test generation for BiCMOS Circuits," *ISCAS*, May 1993, pp. 1714-1717.
74. N. Li and Y.K. Malaiya, "Enhancing Accuracy of Software reliability Prediction" *Proc. IEEE Int. Symp. on Software Reliability Engineering*, Nov. 1993, pp. 71-79.
75. K. Wu and Y.K. Malaiya, "A Correlated Faults Model for Software Reliability," *Proc. IEEE Int. Symp. on Software Reliability Engineering*, Nov. 1993, pp. 80-89.
76. von Mayrhauser, Y.K. Malaiya, P.K. Srimani and J. Keables, "On the Need for Simulation for Better Characterization of Software Reliability," *IEEE Int. Symp. on Software Reliability Engineering*, November 1993, pp. 264-273.
77. S. M. Menon, Y. K. Malaiya and Anura P. Jayasumana, "Faulty behavior of ECL Storage Elements," *Proc. IEEE Int. Workshop on Memory Testing*, August 1993, pp. 31-36.
78. W.K. Alassadi, Y.K. Malaiya and A.P. Jayasumana, "Modeling of Intra-Cell Defects in CMOS SRAM" *Proc. IEEE Int. Workshop on Memory Testing*, August 1993, pp. 78-81.
79. W.K. Alassadi, Ding Lu, A.P. Jayasumana, Y.K. Malaiya and C. Tong, "Faulty Behavior of Asynchronous Storage Elements" *Proc. 5th NASA Symp. on VLSI Design*, Nov. 1993, pp. 7.4.1-7.4.9.
80. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "Limitations of Built-in Current Sensors (BICS) for IDDQ Testing," *IEEE Asian Test Symposium '93*, Nov. 1993, pp. 243-248.
81. N. Li and Y.K. Malaiya, "Fault Exposure Ratio and Reliability Estimation" *Proc. Third Workshop on Issues in Software Reliability*, Nov. 1993, pp. 6.3.1-6.3.18.
82. W. Alassadi, Y.K. Malaiya and A.P. Jayasumana, "Use of Storage Elements as Primitives for Testing Sequential Circuits," *Proc. 6th Int. Conf. on VLSI Design*, Jan. 1993, pp. 118-123.
83. N. Karunanithi and Y.K. Malaiya, "The Scaling Problem for Neural Networks for Software Reliability Prediction" *Proc. IEEE Int. Symp. Soft. Rel. Eng.*, Oct. 1992, pp. 76-82.
84. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "Single BJT BiCMOS Behavior under Stuck and Bridging Faults," *IEEE VLSI Test Symposium*, April 1992, pp. 315-320.
85. W. Alassadi, Y.K. Malaiya and A.P. Jayasumana, "Detection of Feed-Through Faults in CMOS Storage Elements," *Proc. 4th NASA Symp. on VLSI Design*, 1992, pp. 7.2.1-7.2.5.
86. A.K. Anantrao, A.P. Jayasumana and Y.K. Malaiya, "Performance of T1 as an Interconnect of Ethernets Carrying Voice and Data Traffic," *Proc. 26th Ann. Asilomar Conf. on Sig., Sys. and Comp.*
87. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "On Bridging Faults in ECL Circuits," *Proc. 5th Int. Conf. on VLSI Design*, 1992, pp. 55-60.
88. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "Behavior of Faulty Double BJT BiCMOS Logic Gates," *Proc. 4th NASA Symposium on VLSI Design*, 1992, pp. 8.4.1-8.4.12.
89. Y.K. Malaiya, A. von Mayrhauser and P. Srimani, "The Nature of Fault Exposure Ratio," *Proc. IEEE Int. Symp. Soft. Rel. Eng.*, Oct. 1992, pp. 23-32.
90. Y.K. Malaiya, A. von Mayrhauser and P. Srimani, "The Constant Per-Fault Hazard Rate Assumption," *Proc. 2nd Work. Issues in Soft. Rel. Est.*, Oct. 1992, pp. 1-5.
91. Y.K. Malaiya, A.P. Jayasumana, Q. Tong and S. Menon, "Enhancement of Resolution in Supply Current based Testing for Large ICs" *Proc. IEEE VLSI Test Symposium*, April 1991, pp. 291-296.
92. S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "Fault Modeling and Testable Design of 2-level Complex ECL Gates," *Proc. Fourth CSI/IEEE Int. Symp. on VLSI Design*, Jan. 1991, pp. 23-28.
93. N. Karunanithi, Y.K. Malaiya and D. Whitley, "Prediction of Software Reliability Using Neural Networks," *Proc. Int. Symp. on Software Reliability Engineering*, May 1991, pp. 124-130.
94. S. Feng and Y.K. Malaiya, "Evaluation of Detectability in BIST Environment," *Proc. IEEE VLSI Test Symposium*, April 1991, pp. 271-276.
95. R. Rajsuman, A.P. Jayasumana and Y.K. Malaiya, "An Analysis and Testing of Operation Induced Faults in MOS VLSI," *Proc. VLSI Test Symposium*, April 1991, pp. 137-142.
96. Y.K. Malaiya, "Early Characterization of the Defect Removal Process," *Proc. 9th Annual IEEE Software Reliability Symposium*, May 1991, pp. 6.1-6.4
97. J. Bieman, Y.K. Malaiya, K. Olender, R. Oldehoeft and P. Srimani, "The Reliable Software Laboratory at Colorado State University" *Proc. 9th Annual IEEE Software Reliability Symposium*, May 1991, pp. 6.5-6.10.
98. Y.K. Malaiya and P.K. Srimani, "An Introduction to Software Reliability Models," *Proc. CMG-91*, December 1991, pp. 1237-1239.
99. Y.K. Malaiya, N. Karunanithi and P. Verma, "Predictability Measures For Software Reliability Models," *Proc. IEEE Computer Software and Applications Conference (COMPSAC 90)*, Oct. 1990, pp. 7-12.
100. S.M. Menon, A.P. Jayasumana and Y.K. Malaiya, "Gate Level Modeling of ECL Circuits," *Proc. First Great Lakes Symposium*



on VLSI, March 1991, pp. 330-331.

101. Y.K. Malaiya, S. Sur, N. Karunanithi and Y.C. Sun, "Implementation Considerations for Software Reliability," Software Reliability Symposium, June 1990, pp. 6.21-6.30.
102. R. Rajsuman, Y.K. Malaiya and A.P. Jayasumana, "A New Testable Design of Field Programmable Logic Array," *Proc. IEEE Int. Symp. on Circuits and Systems*, 1990, pp. 436-439.
103. S. Hwang, R. Rajsuman and Y.K. Malaiya, "On the Testing of the Microprogrammed Processor," *Proc. 23rd Int. Symp. and Work. on Microprogramming and Microarchitecture*, Nov. 1990, pp. 260-266..
104. A.P. Jayasumana, W. Al-assadi and Y.K. Malaiya, "Pass Transistor Logic Design," in VLSI System Design, Editors: L.M. Patnaik and A.D. Singh, (*Proc. Third International Workshop on VLSI Design*), Tata-McGraw-Hill, Jan. 1990, pp. 13-17.
105. A.B. Kulkarni, Y.K. Malaiya and A.P. Jayasumana, "MESHNET: A New Fault-Tolerant Local Area Network for Industrial Environments," *Proc. 15th Ann. Conf. IEEE Ind. Ele. Soc.*, Nov. 89, pp. 537-542.
106. R. Rajsuman, A.P. Jayasumana and Y.K. Malaiya, "CMOS stuck-open fault detection using single test patterns," *Proc. ACM/IEEE Design Automation Conference*, June 1989, pp. 714-717.
107. P. Verma and Y.K. Malaiya, "In Search of the Best Software Reliability Model," *Proc. 7th Ann. IEEE Software Reliability Symposium*, May 1989, pp. 76-92.
108. Y.K. Malaiya, "On Inherent Untestability of Unaugmented Microprogrammed Control," *Proc. 22nd ACM/IEEE Int. Work. on Microprogramming and Microarchitecture*, August 1989, pp. 88-96.
109. B. Gupta, Y.K. Malaiya, Y. Min and R. Rajsuman, "On Designing Robust Testable CMOS Combinational circuits," *IEE Proceedings*, Vol. 136, Pt. E, No. 4, July 1989, pp. 329-338.
110. Y.K. Malaiya, B. Gupta, A.P. Jayasumana, R. Rajsuman, M. Sankaran and S. Yang, "Functional Fault Modeling for Elementary Static Storage Elements", *IEEE Design For Testability Workshop*, April 1989.
111. Y.K. Malaiya and F. Sheng, "Design of a Testable RISC-to-CISC Control Architecture," *Proc. 21st ACM/IEEE Annual Workshop on Microprogramming and Microarchitecture*, Nov. 1988, pp. 57-59.
112. Y.K. Malaiya, "A Testable and Flexible RISC-To-CISC Control Architecture," *11th Annual IEEE Workshop on Design for Testability*, April 1988.
113. Y.K. Malaiya and P. Verma, "Testability Profile Approach to Software Reliability," in *Advances in Reliability and Quality Control*, Editor: M.H. Hamza, (*Proc. IASTED International Conference on Quality Control and Reliability*), Acta Press, Dec. 1988, pp. 67-71.
114. R. Rajsuman, Y.K. Malaiya and A.P. Jayasumana, "On Accuracy of Switch-Level Modeling of Bridging Faults in Complex Gates," *Proc. 24th ACM/IEEE Design Automation Conference*, June 1987, pp. 244-250.
115. B. Gupta, Y.K. Malaiya, Y. Min and R. Rajsuman, "CMOS Combinational Circuit Design for Stuck-Open/Stuck-Short testability," *Proc. Int. Symp. on Ele. Dev., Cir. and Sys.*, Dec. 1987, pp. 789-791.
116. R. Rajsuman, A.P. Jayasumana and Y.K. Malaiya, "Testability Analysis for Bridging Faults in Dynamic CMOS," *Proc. Int. Symp. on Ele. Dev. Cir. and Sys.*, Dec. 1987, pp. 630-632.
117. Y.K. Malaiya, A. Jayasumana and R. Rajsuman, "A Detailed Examination of Bridging Faults," *IEEE International Conference on Computer Design*, Oct. 1986, pp. 78-81.
118. Y.K. Malaiya, "Options in Control Implementation," *Proc. IEEE International Conference on Computer Design*, October 1985, pp. 267-272.
119. Y.K. Malaiya and S. Yang, "The Coverage Problem for Random Testing," *Proc. International Test Conference*, October 1984, pp. 237-245.
120. Y.K. Malaiya, "Testing Stuck-On Faults in CMOS Integrated Circuits," *Proc. IEEE International Conference on Computer-Aided Design*, November 1984, pp. 248-250.
121. Y.K. Malaiya and R. Narayanaswamy, "Testing for Timing Faults in Synchronous Sequential Integrated Circuits," *Proc. International Test Conference*, October 1983, pp. 560-571.
122. C.C. Liaw, S.Y.H. Su and Y.K. Malaiya, "Self Diagnosis of Non-Homogeneous Distributed Systems," *Proc. 12th International Symposium on Fault-tolerant Computing*, June 1982, pp. 349-352.
123. Y.K. Malaiya and S.Y.H. Su, "A New Fault Model and Testing Technique for CMOS Devices," *Proc. International Test Conference*, November 1982, pp. 25-34.
124. Y. Min, Y.K. Malaiya and S.Y.H. Su, "A Generalization of MTBF for General Digital Systems," *Proc. IEEE International Conference on Circuits and Computers*, September 1982, pp. 220-223.
125. C.C. Liaw, S.Y.H. Su and Y.K. Malaiya, "Detection and Location of Intermittent Faults in Sequential Circuits," *Proc. 11th International Symposium on Fault-tolerant Computing*, June 1981, pp. 244-246.
126. C.C. Liaw, S.Y.H. Su and Y.K. Malaiya, "State Diagram Approach for Functional Testing of Control Sections," *Proc. 1981 International Test Conference*, October 1981, pp. 433-446.
127. Y.K. Malaiya and S.Y.H. Su, "Fault-Tolerance in Multiprocessor Systems", *Proc. IEEE International Conference on Circuits and Computers*, October 1980, pp. 710-716.
128. C.C. Liaw, S.Y.H. Su and Y.K. Malaiya, "Test Generation for Delay Faults using Stuck-at Fault Test Set," *Proc. 1980 Test Conference*, pp. 167-175.
129. Y.K. Malaiya and S.Y.H. Su, "A Survey of Methods for Intermittent Fault Analysis," *Proc. 1979 National Computer Conference*, June 1979, pp. 577-586.

## 6 Abstracts

Yashwant K. Malaiya, "Faults in Microprogrammed and Hardwired Control," Proceedings International Test Conference 1985, USA, November 1985, pp. 732.

## 7 Other Publications (Editorials, invited articles, reports, etc)

1. P.K. Srimani and Y.K. Malaiya, "Steps to Practical Reliability Measurement" (Guest Editors' Introduction), *IEEE Software*, July 1992, pp. 10-12.
2. Y.K. Malaiya, "VLSI Design '92" (Guest Editor's Introduction) *IEEE Design & Test*, Dec. 1992, pp.4-5.
3. Y.K. Malaiya, "Computer Design - G.G. Langdon," *IEEE Design and Test of Computers*, book review, Vol. 2, No. 3, June 1985, pp. 110-111.
4. Y.K. Malaiya, "TC Microprogramming Member Interests tend toward Microarchitecture," *IEEE Computer*, Nov. 1989, 73-74.
5. Y.K. Malaiya, "A Brief History of TC-Micro," *IEEE CS MicroArch*, April 1990, V. 5, No. 1, pp. 25-26.
6. Y.K. Malaiya, "For Diversity, Start 'em Early," *India Abroad*, January 19, 1990, in *Reflections on Life Abroad* column, page 3.
7. Y.K. Malaiya, "Software Reliability Engineering Subcommittee," *Reliability Society Newsletter*, Vol. 36, No. 4, Oct. 1990, pp. 15-16.
8. Y.K. Malaiya, "VLSI Design Symposium," *IEEE Design and Test*, Sept. 1991, pp.78-79.
9. Y.K. Malaiya and M.R. Lyu, "Charter Proposal," *IEEE-CS S. Software Reliability Engineering Newsletter*, April 1991.
10. N. Karunanithi, Y.K. Malaiya and D. Whitley, "Prediction of Software Reliability Using Neural Networks," *SETC Newsletter*, Oct. 1991, pp. vi.
11. Y.K. Malaiya, "Preface" *A Look at Vijayavargia History* by Ranjit Jain, Pub. Vijayavargia (Vaishya) Sabha Gwalior, 1992 (in Hindi, invited)
12. Y.K. Malaiya, "Preservation of Culture" *Saurabh*, Vol. 2, No. 3, July-Sept. 1993, pp. 42-44 (in Hindi).
13. Y.K. Malaiya, "In the Shadow of Hindukush" *Saurabh*, Vol. 3, No. 1, Jan.-March. 1994, pp. 35-37 (in Hindi).
14. Y.K. Malaiya, "On the Shoulders of Giants" In *Three Days' Journey into Self*, YJA, Los Angeles, 2000.
15. Y.K. Malaiya, "Jainism in America," *Lansing Jain Society Pratishtha Souvenir*, 2000, pp.26-29
16. Y. K. Malaiya and Sulekh C. Jain, "Peace through Dialogue," *JAINA 2007 Digest*, pp. 53-57.
17. Sulekh C. Jain and Y. K. Malaiya, "Can Jainism Survive in 21st Century?," *JAINA 2011 Digest*, pp. 125-128.
18. Y.K. Malaiya, "The incredible journey of the 1904 St.Louis Jain temple", *Jain Center of Central Ohio Pratishtha Sovenier*, July 2012, pp. 81-84.
19. Y.K. Malaiya, "As Mumbai Godiji temple celebrates, silence shrouds its predecessor in Pakistan", *Jain Center of Central Ohio Pratishtha Sovenier*, July 2012, pp. 110-112. Also published in *Express Herald Tribune*, Karachi, May 18, 2012.
20. Y.K. Malaiya, The bridge from Ganesh varni to Our times, *Pahali anupasthiti*, Ed. Narendraprakash Jain, Sarojkumar, Satna, p. 25-27, Oct 31, 2013.
21. Y.K. Malaiya, "Dietary Rules in Jainism: A review and Application to Global Society", *Perspectives on the Environment and Sustainable Development in the Four Dharmic Traditions*, Uberoi Foundation, University of Denver. September 30, 2017

## 8 Unpublished Technical Reports

1. P. Wang and Y.K. Malaiya, "Can Anti-random Beat Random Testing? Evaluation from the Randomness Perspective," Tech Report, 2004.
2. C.V. Gupte, A.P. Jayasumana and Y.K. Malaiya, "State Space Exploration of Sequential Circuits for Black-Box testing," Tech. Report, 2003.
3. A.S. Banthia, A.P. Jayasumana and Y.K. Malaiya, "Data-size Reduction for Clustering based Binning of ICs using Principal Component Analysis," Tech. Report, 2003.

## 9 Theses

1. "On Graph-Theoretic Basis for Network Synthesis," M.S. Thesis, Electrical and Electronics Engineering Department, Birla Institute of Technology and Science, Pilani, 73 pages, 1974.
2. "Modeling, Testing and Reliability Analysis of Digital Systems with Intermittent Faults," Ph.D. Dissertation, Department of Electrical Engineering, Utah State University, Logan, 155 pages, 1978.

## 10 Tutorials/Keynotes

1. “Wholistic Engineering for Software Reliability”, Int. Symp. Software Reliability Engineering, 2000.
2. Yashwant K. Malaiya, “Embedded Software Testing”, 35th IEEE VLSI Test Symposium, (VTS 2017), April 2017.

## 11 Invention Disclosures

1. “Single Pattern Testable CMOS (SPT-CMOS) Logic Gates,” by R. Rajsuman, A.P. Jayasumana and Y.K. Malaiya, 1988.
2. “TCMOS: Testable CMOS Logic Gates,” by A.P. Jayasumana, Y.K. Malaiya, R. Rajsuman, 1989.
3. “A Design for Testability scheme for detection of stuck-open faults in single BJT BiCMOS Logic devices.” S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, 1992.
4. “BiCMOS Domino: A Novel High-Speed Dynamic BiCMOS Logic Family,” A.P. Jayasumana, Y.K. Malaiya and S.M. Menon, 1993
5. “Identification and Binning of Faulty ICs Using Principal Component Analysis,” A. Sharma, A.P. Jayasumana and Y.K. Malaiya, 2005.

## 12 Advising: Graduate committees (partial list)

I have **advised more than 65** graduate students and have **served on the committees for more than 250** graduate students at Colorado State University. The list below lists the graduate students who have finished (since 2003 only).

Ph.D.(as advisor/coadvisor) : Omar Alhazmi, HyunChul Joh, Sopak Chaichana, Ruyi John Fan, Awad Younis, Abdullah Algarni.

Ph.D.(as committee member) : Ibrahim Lazrig, Mustafa Al-Lail, Mozammel Hossain, Sai Vineel Reddy Chittamuru, Mustafa Al-Lail, Kiril Belyaev, Negar Mosharraf Ghahfarokhi, Lijun Yu, Wedyan, Fadi Ibrahim , Abdunabi, Ramadan Farag, Fahad Al Zahrani, Zhou Dacheng, Abdulgader Habibulla, Alkan Cengiz, Ayman Fayumi, C.R. Rose, Dan Vivanco, Dinh Trong Trung, H Nasser, Huxia Wang, Nischal Piratla, J S Tamez, Pan Ho Lee, Henry Dittmer, Sudip Chakraborty, Woo Sung-whan, Sangeeta Bangalore, Yoong Goog Cho.

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## 13 Research projects (as principal investigator)

- *Modeling, Testing and Fault-tolerant Design of Digital Systems with Intermittent Faults*, National Science Foundation, 1979-1981, \$110,006, (with S.Y.H. Su)
- *Testability for VLSI*, Rome Air Development Center, 1981-1982, \$40,000, (with S.Y.H. Su)
- *Functional Testing of LSI/VLSI based Systems with Measures of Fault Coverage*, Department of the Army (USACECOM) 1982-1984, \$158,808, (with S.Y.H. Su), associated until August 1982.
- *Reliability Management Through Self-Testing*, Office of Naval Research (SDIO/IST), 1986-1988, \$271,198,
- *Reliability Management Through Self-Testing*, (Renewal), Office of Naval Research (SDIO/IST) 1989-1991, \$269,518.
- *Reliability Management Through Testing*, Office of Naval Research (SDIO/IST) 1992-1996, \$317,618
- *Achieving Ultra High Reliability in Critical Systems*, Office of Naval Research (BMDO), 1996-1999 \$272,990
- *An Integrated Software Reliability Tool*, (ONR/AASERT), 1996-1999 \$108,424
- *Achieving Introducing Computer Science, A Summer Program*, Colorado Institute of Technology, 2001, \$20,000 (with S. Ghosh and S. Schleiffers).