Limitations of Built-In Current Sensors (BICS) for I_{DDQ} Testing*

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Abstract

Quiescent current (I_{DDQ}) drawn by a static CMOS device is extremely small and is of the order of nanoamperes. Under many faults, I_{DDQ} can increase by several orders of magnitude. Either an external or an on-chip current sensor can be used to detect enhanced static current drawn by a static CMOS device. An on-chip sensor, termed a BICS (Built-In Current Sensor) can be significantly faster. Implementation of BICS has received a lot of interest in the recent years.

Some limitations posed by BICS on I_{DDQ} measurement caused due to increase in I_{DDQ} settling time as well as propagation delay is considered. Results indicate that careful attention needs to be given to circuit partitioning for implementing BICS. Some of the considerations that need to be taken into account while designing new BICS are presented.

1 Introduction

The use of leakage current measurement to detect faults in CMOS ICs has been under consideration for a number of years [1]. Recent studies on leakage current based testing techniques, [2], [3] have concluded that it is necessary to include I_{DDQ} monitoring to obtain highly reliable CMOS ICs. The data presented for four sample CMOS ICs showed that the defect detection increased between 60% to 180% when I_{DDQ} monitoring is added to a functional test set [2]. For I_{DDQ} monitoring, either an external (off-chip) or an on-chip current sensor can be used. On-chip current sensor or a Built-in Current Sensor (BICS) can be significantly faster than the off-chip sensor.

In Section 2, we review the research on current testing. In Section 3 we discuss partitioning of a circuit for the purpose of improving the resolution of the current testing. BICS and its limitations are presented in sections 4 & 5 respectively. We conclude in Section 6.

2 Background

There are several reasons for using I_{DDQ} monitoring for testing of ICs [4], [5]. Traditional IC testing techniques are not effective in detecting a number of failure modes in CMOS ICs. In general, faults such as gate oxide shorts [4, 7], certain bridging faults [8, 9], certain open faults, stuck-on faults [6], punch-through faults, operation induced faults [10], parasitic devices, pn junction leakage, and abnormally high contact resistance, may not manifest as logic faults and therefore will not be detected by traditional tests which monitor the output logic levels. These localized defects degrade the electrical performance of the circuit without affecting the logical operation performed by the circuit.

A major fraction of failures caused by circuit fatigue will first appear as parametric drifts. Progressive gate oxide leaks for example, may not initially affect the functionality of a device, but could become shorts during a short time leading to the failure of a device [6]. Eventually some of them will advance enough to alter the

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logical behavior or circuit failure. Leakage current based testing will detect these parametric drifts before they actually change the circuit behavior. Data exists that show that a device that fully passes the logic functional tests but fail the I_{DDQ} test, fall in a significant category that functionally fail more frequently in early life than normal [4].

The off-chip current testing has several other advantages over the traditional functional testing techniques [1]. In functional testing, the site of a fault has to be excited and the effect of the fault has to be propagated to the output. In I_{DDQ} testing, the propagation of the effect is automatic. Further, it can provide transistor level resolution as opposed to gate level resolution. Off chip current testing has proved to be very efficient for circuits like static RAMs [11].

Stuck-on faults in CMOS circuits cannot be detected using traditional functional fault testing techniques. Test generation for detection of such faults, when I_{DDQ} testing is used, is considered in [12]. Different decision processes involved in detecting such faults have been examined. The voltage level under stuck-on or bridging faults in CMOS circuits depend on the relative impedances of the transistors involved and the bridge [13]. This makes detection of such faults difficult using voltage measurement techniques. However, I_{DDQ} testing detects such faults. It has been shown that I_{DDQ} testing also detects multiple stuck-at faults as well as logically redundant faults [13], [14].

I_{DDQ} testing was demonstrated to reduce line fallout after 99.6% stuck-at fault testing failed to achieve desired quality goals [15]. The high resolution required for current testing has been cited as another problem that makes acceptance of current testing difficult at present [3].

The key to performing an effective I_{DDQ} test is the probe circuit used to measure the current. Such a circuit should be capable of measuring small currents, without affecting the supply voltage especially during transients, and must be capable of fast measurements [16]. The different types of current probes in use are examined in [16], and a probe circuit has been proposed which allows a system to perform dynamic I_{DDQ} tests as an integral part of the functional testing of a CMOS device.

Built-in current sensing techniques have been proposed to overcome the disadvantages of existing off-chip current testing techniques. Current sensors have been proposed and implemented using CMOS technology, some capable of detecting currents as small as $2\mu a$ at 1MHz clock frequency [3], [4]. In BIC testing, an IC is implemented using a number of modules and each module is connected to the power supply through a current sensor. Another circuit design for built-in current testing has recently been proposed [17]. The output of the current sensor of a module is observed with the proper input vectors to detect faults in that particular module. Limitations of BIC sensors due to virtual ground is considered in section 4.

3 Partitioning Large Circuits

For large circuits, it would be difficult to distinguish the faulty current from the normal one. The solution to this problem will be to partition the device under test into modules. Each module will have its own current sensor. Thus these modules can be tested independently. A statistical characterization is presented in [18, 19]. The size of each module can be controlled such that the faulty and normal distributions within each module can be distiguished.

An upper bound of maximum n, denoted by n_b has been arrived at in [18, 19], where n is the number of cells in one module. Hence, the device can be partitioned into modules whose sizes will not exceed n_b, and all the modules will have approximately the same number of cells.

There is another reason why we want to partition the device into several modules. The larger the device or circuit becomes, the larger the capacitance there will be at the current sensor input. So it will take longer period for the current sensor to respond to show the value of the current flow in the circuit. The speed is limited due to the fact that the current monitoring has to be done after the transients have died down. The duration of the transients will depend among other things on the capacitance associated with measurement points. Thus the larger the circuit that is covered by a current monitor, the longer will be the transient time.

4 Built-In Current Sensors

The simplest current sensor can be built with either a resistive or a capacitive element (labeled I-V Converter in Figure 1) along with a voltage comparator, as shown in Figure 1. The current flow will cause a voltage drop on the I-V converter element and the voltage on node VG(Virtual Ground) is fed to the comparator [16], [21].

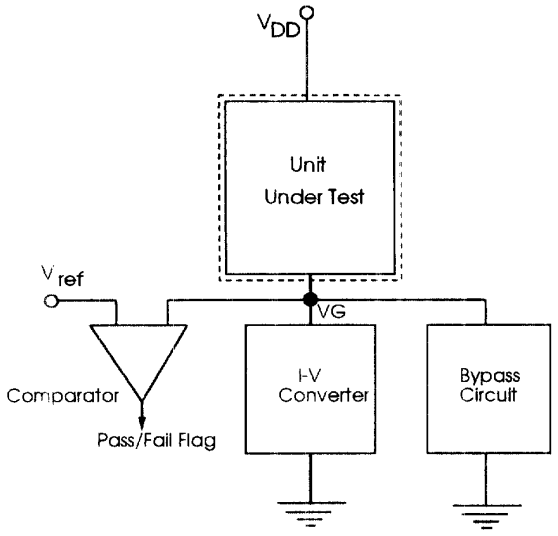

Figure 1: A general current sensor

The other input of the comparator is the standard voltage (V_{ref}) which would result from I_{DDQth}. Therefore, if the measured current I_{DDQ} is greater than I_{DDQth}, the output of the current sensor is 1. If I_{DDQ} is equal to or smaller than I_{DDQth}, the output of the current sensor is 0.

Since each module or subcircuit has its own current sensor, it is impractical to observe the output of every current sensor. One solution to this problem is to propagate the outputs of all the sensors to one observable output pin which is designed solely for making pass/fail decision. This can be implemented by using an OR gate. The outputs from all the current sensors are fed to the OR gate. When the current drawn by one or more modules exceed I_{DDQth}, the output of the OR gate changes state. Thus, detecting enhanced I_{DDQ}.

5 Limitations Of BICS

For I_{DDQ} monitoring, the measurement of the supply current has to be performed by the current sensor after the initial transients have died down. Figure 2 shows a plot of I_{DD} vs. Time for a CMOS circuit. t_{pdmax} is caused due to the initial transients in the supply current due to switching in the various gates of the CMOS circuit. It takes certain amount of time (t_c) for the current tail to end, i.e., the current to settle to an almost constant value of the order of pico or nano Amps in a fault-free CMOS circuit. In a faulty CMOS circuit, the

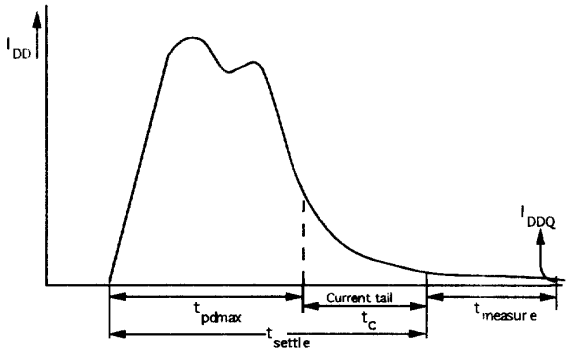

Figure 2: Plot illustrating I_{DD} vs. Time for a CMOS circuit

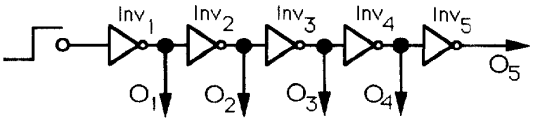

Figure 3: An inverter chain with 5 inverters

value of I_{DDQ} can be a few orders of magnitude greater than the fault-free I_{DDQ} value. The total time taken for the current to settle (t_s) is the sum of t_{pdmax} and t_c.

Consider the inverter chain (5-level) consisting of 5 inverters shown in Figure 3. Input/Output waveforms along with current (I_{DD}) waveform obtained using SPICE simulations are shown in Figure 4. The current waveform shows almost ≈0.4mA current drawn by the 5 inverter chains when the gates are switching. The last gate (Inv_5) switches around 9.2ns, shown as t_{pd} in the plot. After the last gate switches, the current goes to a steady low current in a fault-free CMOS circuit. The time from when the last gate switches (t_{pdmax}) and until the current reaches the steady low current value is termed as t_c. The sampling of the supply current can be done any time after the current tail has reached the almost fixed very low value of current in fault-free CMOS circuit. If the CMOS circuit is faulty, then the current at this time would be elevated and hence the BICS would be able to detect the fault. This results in a settling time of $t_{settle} = t_{pdmax} + t_c$.

One of the components of the settling time t_{settle} is t_{pdmax} and the other component is t_c caused by the current tail. t_{pdmax} can be obtained directly from the max-

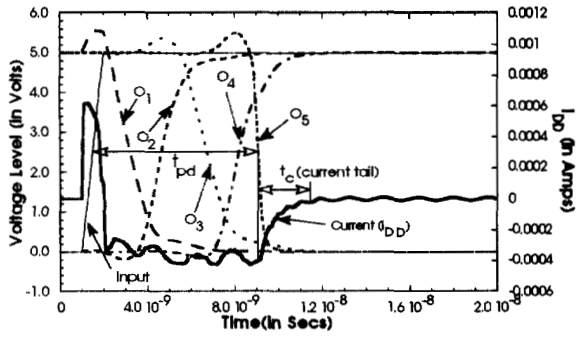

Figure 4: Input/Output & current waveforms for inverter chain with 5 inverters

imum propagation delay of the complete chain of the gates in a given circuit. The second component t_c of the settling time caused by the current tail depends on the rise-time (t_r) and fall-time (t_f) of the last few gates of the circuit, Capacitance (C), BICS Resistance (R') and the distribution of propagation delays (D_{pd}) amongst the various levels of the circuit.

CMOS circuits with varying number of gates were simulated using a built-in current sensor (BICS) [3] as shown in Figure 5 to study the settling time of the power supply current. CMOS circuits of different levels (1,3, 5 and 10 levels) were chosen for simulation with BICS (Built-in Current Sensor) to determine the time for current to settle. The number of levels indicate the number of gates connected in series with one another. For example, simulation for 5 levels totaling 500 gates has 5 gates connected in series with 100 such series of gates in parallel. Figure 6 shows plots for I_{DDQ} settling time vs. total number of gates for different levels of CMOS circuits. The current is sampled by the BICS only after all the transients due to switching have completed and the current has settled to a steady low current value [3]. The settling time shown in Figure 6 shows the time when the current has settled to about 5% of the steady low current value for sampling by the BICS. The settling time for a 10-level circuit for example, is greater than that of a 5-level circuit with the same number of gates due to the larger propagation delay (t_{pd}) in the former. For a circuit with a given level, the settling time increases with the number of gates. The settling time thus has two components, one due to the propagation delay, and the other due to the capacitance at the node to which the current sensor is connected. Thus the larger the circuit that is covered by a current monitor, the longer the second component of the transient time will be. Another advantage of partitioning is the reduction of this component of settling time due to the total capacitance. In addition to the increase in I_{DDQ} settling time with increasing gates for a given fixed level, the propagation delay (t_{pd}) also increases with increasing number of gates, as the capacitance seen by the BICS increases with increasing number of gates (transistors). It may be noted that when BICS is not implemented or when the virtual ground is connected to the physical ground, I_{DDQ} settling time for a circuit with a certain number of levels remains fixed. The I_{DDQ} settling time does not increase with increasing number of gates as the effect due to capacitance (C) caused by the circuit under test as well as due to BICS resistance (R') do not exist.

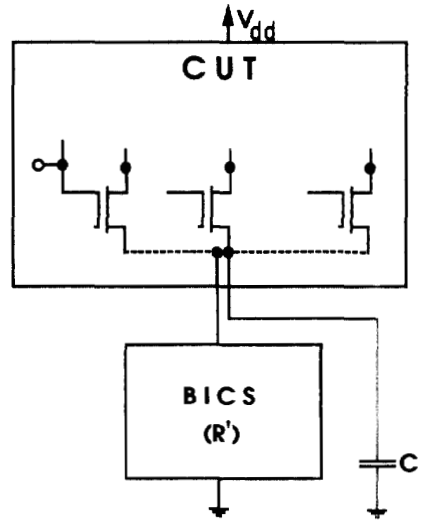

Figure 5: CMOS circuit with BICS

When BICS is implemented the transistor terminals (source or drain) in a CMOS circuit which otherwise would have been connected to ground is connected to the BICS. The transistor terminal (source or drain) capacitance (C) of all the transistors appears as one lumped capacitance at the input of the BICS. The larger the circuit under test (CUT), the larger the capacitance seen by the BICS.

The settling time (t_{settle}) of current for a given CMOS circuit as shown in Figure 6 is a function of the following:

$$t_{settle} = mt_{pd} + R'C(f(D_{pd}, t_r/t_f))$$

where m = the maximum number of levels in a given CMOS circuit,

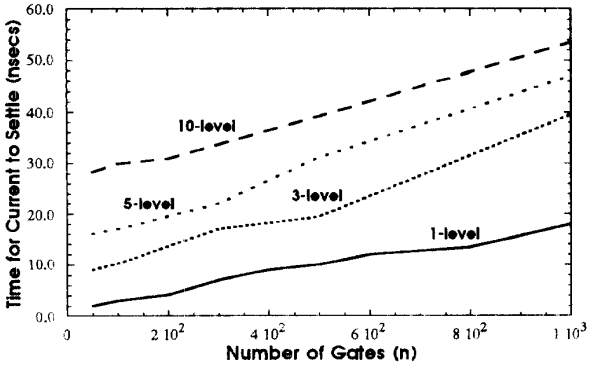

Figure 6: I_{DDQ} settling time vs. Number of gates for different levels

n = the number of gates in a given CMOS circuit,
C = total capacitance of the V_{DD} or Ground rail of CUT connected to BICS,
R' ◻ denotes the effect due to BICS resistance,
t_r / t_f = rise-time or fall-time of the gate switching towards the end.
D_{pd} = Distribution of propagation delays amongst the various levels of the circuit.

To assess the effects of the capacitance (C) of the circuit under test and the resistance of the BICS (R') on the settling time for I_{DDQ} measurement, simulations were carried out and the results are given below. For varying the capacitance seen by the BICS and to estimate the effects on settling time, a circuit with 10 level inverter chain was chosen and the capacitance (C) seen by the BICS was changed to simulate for gates upto 1000 gates and the plot obtained is shown in Figure 7. The above simulations show increasing I_{DDQ} settling time with increasing capacitance seen by the BICS. Effects of the BICS resistance (R') was simulated by replacing the BICS with a resistance. The value of the resistance was varied from 10Ω to 10000Ω and the effects on I_{DDQ} settling time as well as on the propagation delay of the inverter chain is shown in Figure 8. Results indicate increasing I_{DDQ} settling time as well as increasing propagation delay with increasing BICS resistance (R').

With the above results, the partitioning of a given circuit becomes very critical as the capacitance offered at the input of BICS also needs to be considered. in addition to the area overhead and resolution of the BIC sensor. The effect of the capacitance (C) on BICS resulting in additional propagation delay of the CMOS circuit is an-

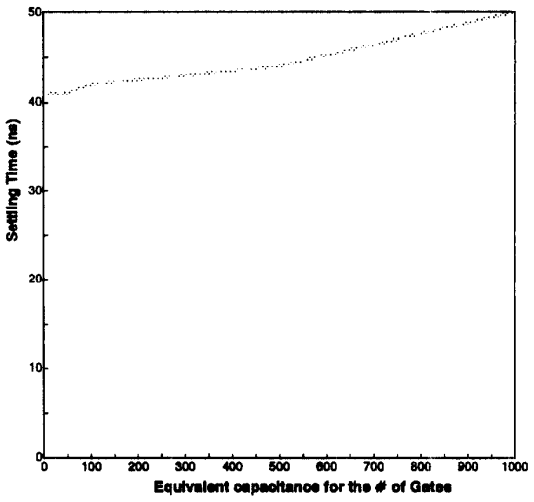

Figure 7: I_{DDQ} settling time vs. Equivalent Capacitance (C) for # of gates

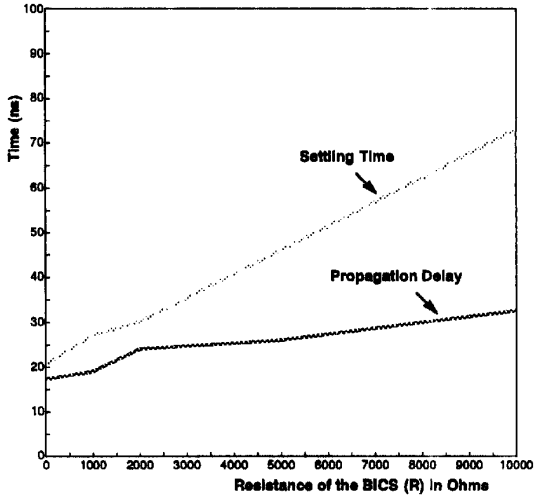

Figure 8: I_{DDQ} settling time & Propagation delay vs. BICS Resistance (R')

other problem caused by the BICS. This can be avoided by providing a physical ground pin in addition to the virtual ground pin. This facilitates the ground pin to be connected to the ground terminal of the system and hence avoiding the propagation delay introduced in the circuit by the BICS. This scheme provides Off-line BICS, wherein whenever current sensing is required to be carried out, the BICS is introduced into the circuit by disabling the ground pin and making it virtual ground.

6 Conclusions

Testing of larger ICs using I_{DDQ} monitoring requires larger test times and exhibits lower resolution between faulty and fault-free devices. Some limitations caused by BICS posed by virtual ground on the measurement of I_{DDQ} is shown. Careful partitioning of large circuits may be required to reduce the effects of virtual ground caused by BICS. Also, use of an additional pin to avoid the propagation delay effects of BICS on the circuit under test is suggested.

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