Testable Design of BiCMOS Circuits for Stuck-Open Fault Detection Using Single Patterns

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Abstract—**Single BJT BiCMOS devices exhibit sequential behavior under transistor stuck-OPEN (s-OPEN) faults. In addition to the sequential behavior, delay faults are also present. Detection of s-OPEN faults exhibiting sequential behavior needs two-pattern or multipattern sequences, and delay faults are all the more difficult to detect. A new design for testability scheme is presented that uses only two extra transistors to improve the circuit testability regardless of timing skews/delays, glitches, or charge sharing among internal nodes. With this design, only a single vector is required to test for a fault instead of the two-pattern or multipattern sequences. The testable design scheme presented also avoids the requirement of generating tests for delay faults.**

I. Introduction

COMBINING the advantages of CMOS and bipolar, BiCMOS is emerging as the major technology for many high performance digital and mixed signal applications. The main advantages of CMOS technology over bipolar are lower power dissipation and higher packing density [1].

Bipolar technology offers better output current drive, switching speed, I/O speed, and analog capability. Combining the advantages of bipolar and CMOS, BiCMOS offers the following advantages [1]: improved speed over CMOS, lower power dissipation compared to bipolar, flexibility in I/O (TTL, ECL, CMOS compatibility), high performance analog capability, and latch up immunity. BiCMOS is even being considered for high performance microprocessors and dynamic RAM's, and it is felt that it will be one of the main technologies to drive almost all functions in the decade ahead [2].

Most of the defects and failures in present day integrated circuits can be abstracted to shorts and opens in the interconnects and degradation of devices [3]. Transistor level shorts and opens model many of the physical failures and defects in IC's [3]. A study by Gailiay [4] on 4-b MOS microprocessor chips revealed that many of the faults were shorts and opens at the transistor level. Analysis of faults in elementary static storage elements suggest that transistor level testing provides a higher coverage of faults compared to that at the gate level [5]. The major fault models at transistor level are stuck-at faults, and shorts and opens of transistors and interconnects [6]. It has been shown that the stuck-at model does not cover many of the manufacturing defects in BiCMOS devices and that most open faults manifest themselves as delay faults [7], [8].

BiCMOS circuits employ one or two bipolar junction transistors (BJT's) to perform the function of driving output loads and CMOS to perform logic functions. The BiCMOS NAND realization used in this study uses a single BJT (S-BJT) in the output stage. Stuck-Open (s-OPEN) faults in S-BJT BiCMOS devices can exhibit sequential behavior or delay fault [8]. Detection of such sequential behavior due to s-OPEN faults in CMOS requires two pattern tests instead of a single pattern [4], [9]–[11]. The first pattern is applied to initialize the output of the gate and the second pattern to detect the fault [12], [13]. For detection of an s-OPEN fault in the p-part(n-part), the first pattern sets the output to logic ZERO (logic ONE). The second pattern then attempts to provide a low-resistance path between the output and the power-supply (ground) through the faulty transistor. To avoid invalidation of tests in the presence of timing skews, two-pattern tests have been suggested. In such two-pattern sequences, the Hamming distance between the initialization pattern and the second test pattern is kept at unity [14]–[16], so as to avoid the possible intermediate state.

The generation of two-pattern test sequences is a complex process. The requirement of large CPU time makes the test generation process expensive. It is also possible that a two-pattern sequence may not exist for certain faults in a combinational circuit [14], [15]. Testable design schemes employ extra transistors in fully CMOS (FCMOS) gates and augment CMOS circuits to detect s-OPEN faults. The test generation complexity for these circuits is less compared to that of FCMOS circuits. However, the above augmented circuits also require two-pattern or multipattern test sequences. Certain conditions under which the schemes proposed in [14], [15], [17], [18] fail to detect s-OPEN faults is presented in [19]. Testable designs for CMOS devices to detect s-OPEN using a single test vector in the presence of glitches and timing skews were presented in [19], [20]. S-BJT BiCMOS devices under s-OPEN faults manifests either as sequential behavior or

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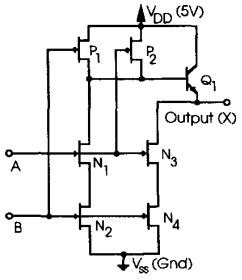

Fig. 1. An S-BJT BiCMOS NAND.

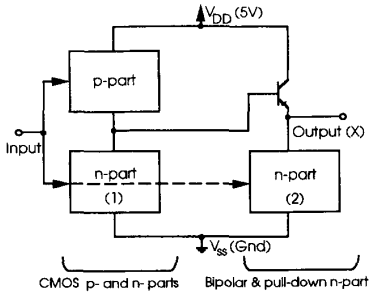

Fig. 2. A general S-BJT BiCMOS device.

as delay faults. Detection of s-OPEN faults causing sequential behavior can be carried out using the methodologies mentioned above for CMOS devices. Testing of delay faults also require two-pattern tests.

In this paper, we first examine the operation of S-BJT BiCMOS NAND device under s-OPEN faults. A testable scheme is proposed to detect s-OPEN failures in S-BJT BiCMOS devices using single test vector. Sections II and III deal with description of functioning of BiCMOS devices and analysis of s-OPEN failures in S-BJT BiCMOS devices, respectively. In Section IV, we show invalidation of two-pattern and multipattern test sequences under glitches and timing skews. Sections V and VI deal with robust testable BiCMOS design and their advantages, respectively.

II. BiCMOS Devices

S-BJT BiCMOS NAND realization is shown in Fig. 1. The functioning of the BiCMOS NAND can be explained as follows: Applying logic "0" to one or both of the inputs would cause at least one P-device to be ON and at least one N-device in each serial N-pairs to be OFF. With the P-devices (P_1 and/or P_2) ON, the base of the bipolar NPN transistor would be about 5 V, thus supplying a base current and turning ON the bipolar transistor to provide logic "1" at the output. Either of the inputs at logic "0" and the other input at logic "1" would still cause either of the parallel connected P-devices to be ON and either of the series connected N-devices to be OFF. This would still cause logic "1" at the output. With both the inputs at logic "1," the P-devices (P_1 and P_2) would be turned OFF, and the N-devices N_1, N_2, N_3, and N_4 would be turned ON causing a conduction path from output node to ground. This will cause the output to be logic "0." Thus, the circuit realizes the NAND function. S-BJT BiCMOS devices do not have the full V_{DD} to Ground logic swing of CMOS devices. The output "high" voltage (V_{OH}) is limited to V_{DD}–$V_{BE(Q1)}$. However, output "low" voltage (V_{OL}) is $\approx$ 0 V. The logic levels for BiCMOS are 0 to 0.8 V for logic level "0" and 2.4 to 5 V for logic level "1" [21]. Any voltage between 0.8 and 2.4 V is considered indeterminate. These values are consistent with Fujitsu [22] BiCMOS ASIC DC characteristics of $V_{IL\,\max} =$ 0.8 V and $V_{OH\,\min} = 2.4$ V. Block diagram of a general S-BJT BiCMOS device is shown in Fig. 2. An S-BJT BiCMOS gate consists of CMOS p- and n-parts to perform logic function and a BJT and a pull-down n-part for driving the output node.

TABLE I
Behavior of BiCMOS NAND with s-OPEN Faults

BiCMOS NAND Stuck-OPEN results										
Input	*ff*	P_1^{OP}	P_2^{OP}	N_1^{OP}	N_2^{OP}	N_3^{OP}	N_4^{OP}	Q_{1e}^{OP}	Q_{1b}^{OP}	Q_{1c}^{OP}
A B	X	X	X	X	X	X	X	X	X	X
0 0	1	1	1	1	1	1	1	R	R	D_{0-1}
0 1	1	1	Q^n	1	1	1	1	R	R	D_{0-1}
1 0	1	Q^n	1	1	1	1	1	R	R	D_{0-1}
1 1	0	0	0	D_{1-0}	D_{1-0}	S	S	0	0	0

X = Output, *ff* = fault free, D_{1-0} = High to Low transition Delay Fault, (e, b, c = emitter, base, collector), D_{0-1} = Low to High transition Delay Fault, N_1^{OP} = Transistor N_1 Open, Q^n = Previous State, S = Stuck-at-1 after initialization (Special case of Q^n), R = Stuck-at-0 after initialization (Special case of Q^n).

III. Analysis of Stuck-Open Failure

In this section, the response of the BiCMOS NAND is evaluated for s-OPEN failures of the bipolar and MOS transistors. The output of the BiCMOS gate is obtained by simulating one failure at a time for all possible s-OPEN failures of all transistors. The s-OPEN failures in pMOS and nMOS were simulated by turning OFF the respective transistors. Open in bipolar transistor terminals (emitter, base, and collector) were simulated by connecting a resistance of $R > 1$ MΩ in series with the corresponding node.

The fault-free and faulty behavior [8] of BiCMOS NAND is summarized in Table I. The length and width of pMOS (L_p, W_p) and nMOS (L_n, W_n) transistors used for BiCMOS devices in this study are ($L_p = 1.5\,\mu$m, $W_p = 30\,\mu$m) and ($L_n = 1.5\,\mu$m, $W_n = 26\,\mu$m), similar to the values used in [7] for consistency. In Table I, the subscript represents the transistor number for the BiCMOS circuit shown in Fig. 1, and superscript represents the type of hard failure under consideration where OP indicates s-OPEN failure. For example, N_1^{OP} indicates transistor N_1 s-OPEN, and Q_{1c}^{OP} indicates transistor Q_1 collector open.

In order to make the analysis a true representative of circuit conditions, CMOS inverters were used to drive the BiCMOS device, and CMOS inverters were used as load to the BiCMOS device as shown in Fig. 3. Gates G_1 and G_2 are CMOS inverters used to drive the BiCMOS NAND gate G_3. CMOS inverter G_4 is used as load to the BiCMOS NAND. The length and width of pMOS (L_p, W_p) and nMOS (L_n, W_n) transistors used as CMOS load and driver devices in this study are the same as the BiCMOS device length and width. The resistance and capacitance values used in the SPICE parameters for

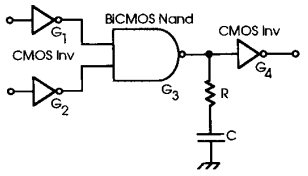

Fig. 3. S-BJT BiCMOS NAND with CMOS inverter load and driver.

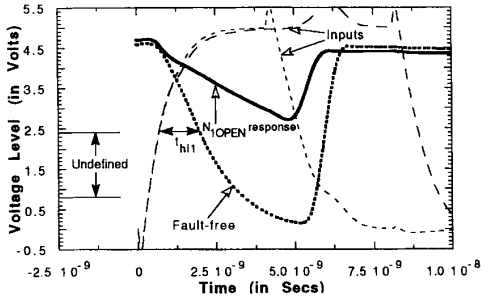

Fig. 4. BiCMOS response to N_1^{OPEN} with t_{pw} = 4 ns and *RC* load.

BJT and MOSFET transistors are (BJT: $R_E = 10\,\Omega$, $R_B = 50\,\Omega$, $R_C = 20\,\Omega$, $C_{JE} = 40e-15$, $C_{JC} = 33e-15$), (pMOS: $C_J = 1.5e-4$, $C_{JSW} = 8e-10$, $C_{GSO} = 0.493e-9$, $C_{GDO} = 0.493e-9$) and (nMOS: $C_J = 2.3e-4$, $C_{JSW} = 92$–10, $C_{GSO} = 0.493e-9$, $C_{GDO} = 0.493e-9$). To study the effects of output fan-out on BiCMOS devices, analysis was conducted with one CMOS load alone and also with an *RC* ($R = 100\,\Omega$, $C = 1$ pF) load along with a CMOS load as shown in Fig. 3.

Description of faulty behavior with respect to different kinds of faults in S-BJT BiCMOS NAND is given in [8]. Here, we are concerned only with s-OPEN faults.

A. The s-OPEN Faults in BiCMOS

The s-OPEN failure of transistor N_1 or N_2 exhibit unique delay fault. A first glance would lead one to expect that with input vectors 11, the output parasitic capacitance would be discharged by transistors N_3 and N_4 turning ON. However, due to the open fault of transistor N_1 (or N_2) under consideration, the vectors 00, 01, or 10 would charge up the parasitic capacitors at the base as well as the emitter nodes of the bipolar transistors. With the application of input vector 11, the series path of N_3 and N_4 will be turned ON, but the series path of N_1 and N_2 will not be turned on due to the fault. This will cause transistor Q_1 to remain ON for sometime because of the charge stored at the base of the bipolar transistor. The base voltage will decay through the ON resistance of N_3 and N_4 under vector 11, causing delay in the output response. This delay fault in 1-to-0 transition is shown in Fig. 4. This type of fault has also been observed in [7] for a different implementation of a BiCMOS NAND gate.

Fig. 4 shows the response of BiCMOS NAND to N_1^{OP} with one CMOS load connected to the BiCMOS output and with input pulse width $t_{pw} = 4$ ns, where the faulty output does not have time enough to go below noise margin of logic "1"

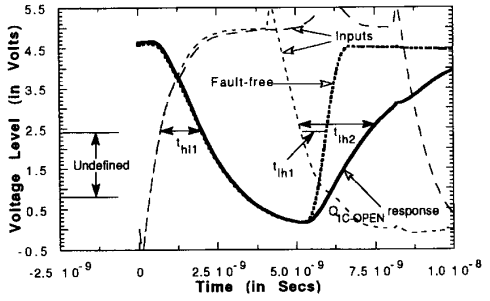

Fig. 5. BiCMOS response to Q_{1C}^{OPEN} with $t_{pw} = 4$ ns and *RC* load.

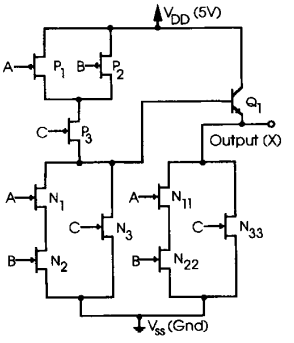

Fig. 6. S-BJT complex BiCMOS gate realizing the function $f = \overline{A.B + C}$.

range. Before the output can go below logic "1" range, the input undergoes 1-to-0 transition causing the output to change state and become logic "1."

Bipolar transistor emitter and base s-OPEN faults manifest as stuck-at-0 after initialization (shown as R in Table I). It can be seen that with either of the above faults, output cannot go to logic "1" (other than during power up) as no path exists between output and V_{DD}. With collector open, the output exhibits low-to-high transition delay ($D_{0\text{-}1}$) as shown in Fig. 5. Fig. 5 shows the response of BiCMOS NAND to transistor Q_1 collector open with one CMOS load connected to the BiCMOS output and with input $t_{pw} = 4$ ns, where the faulty output exhibits larger delay for the low-to-high transition. The faulty low-to-high transition delay was seen to be $t_{lh2} = 2.4$ ns instead of the normal low-to-high transition delay of $t_{lh1} = 0.91$ ns.

B. The s-OPEN Faults in Complex S-BJT BiCMOS Gate

Based on the s-OPEN failure analysis on BiCMOS NAND, s-OPEN faults in a complex S-BJT BiCMOS gate were analyzed. The complex S-BJT BiCMOS device shown in Fig. 6 realizes the function $f = \overline{A.B + C}$. The fault-free and faulty behavior of the complex S-BJT BiCMOS gate is given in Table II. This complex gate is later used as an example to show the test invalidation of two pattern or multipattern test sequences if the inputs to this gate are affected by glitches caused by timing skews/delays. The s-OPEN faults of pMOS transistors and nMOS transistors (N_1, N_2 and N_3) manifest as sequential behavior (Q_n) and high-to-low delay

TABLE II
BEHAVIOR OF COMPLEX S-BJT BiCMOS GATE WITH s-OPEN FAULTS

Complex S-BJT BiCMOS Gate Stuck-OPEN results													
Input	ff	P_1^{OP}	P_2^{OP}	P_3^{OP}	N_1^{OP}	N_2^{OP}	N_3^{OP}	N_{11}^{OP}	N_{22}^{OP}	N_{33}^{OP}	Q_{1e}^{OP}	Q_{1b}^{OP}	Q_{1c}^{OP}
A B C	X	X	X	X	X	X	X	X	X	X	X	X	X
0 0 0	1	1	1	Q^n	1	1	1	1	1	1	R	R	D_{0-1}
0 0 1	0	0	0	0	0	0	D_{1-0}	0	0	Q^n	0	0	0
0 1 0	1	Q^n	1	Q^n	1	1	1	1	1	1	R	R	D_{0-1}
0 1 1	0	0	0	0	0	0	D_{1-0}	0	0	Q^n	0	0	0
1 0 0	1	1	Q^n	Q^n	1	1	1	1	1	1	R	R	D_{0-1}
1 0 1	0	0	1	0	0	0	D_{1-0}	0	0	Q^n	0	0	0
1 1 0	0	0	1	0	D_{1-0}	D_{1-0}	0	Q^n	Q^n	0	0	0	0
1 1 1	0	0	0	0	0	0	0	0	0	0	0	0	0

X = Output, ff = fault free, D_{1-0} = High to Low transition Delay Fault,
(e, b, c = emitter, base, collector), D_{0-1} = Low to High transition Delay Fault,
N_1^{OP} = Transistor N_1 Open, Q^n = Previous State,
R = Stuck-at-0 after initialization (Special case of Q^n).

($D_{1\text{-}0}$), respectively. The s-OPEN faults of nMOS transistors (N_{11}, N_{22}, and N_{33}) result in sequential behavior (Q_n).

Transistor Q_1 emitter or base open faults manifest as stuck-at-0 after initialization (R) where the output cannot go to logic "1" (other than during power up) as no path exists between output and V_{DD}. With Q_1 collector open, the output exhibits low-to-high transition delay ($D_{0\text{-}1}$).

IV. GLITCHES AND TIMING SKEWS

Two-pattern or multipattern sequences are applied for detection of s-OPEN faults manifesting as sequential behavior. Two-pattern or multipattern test sequences lead to invalidation of tests if the inputs to a gate are affected by glitches caused by timing skews/delays. An example illustrating formation of glitches due to timing skews/delays in the prior logic is shown in [19], [21]. Several other factors also could cause glitches, such as, due to switching of some transistors, external electromagnetic interference, ionization radiation, etc. Testability of a circuit may be affected drastically by the presence of glitches.

A. Performance of BiCMOS in the Presence of Glitches

Failure of robust test sequences is illustrated in the presence of glitches. The following definitions are used in this paper:

Definition 1: A glitch will be called *negative(positive)* if the steady state voltage level at line/node of interest is logic *ONE* (logic *ZERO*) and goes to logic *ZERO* (logic *ONE*) momentarily because of the glitch. The presence of a glitch will be denoted by G_l.

Definition 2: A *Zero Vertex* 0Vx (*One Vertex* 1Vx) is an input vector to a logic gate, which produces an output logic value *ZERO*(*ONE*) in the fault-free gate.

Definition 3: A *RobustH1 test sequence* is a sequence of two or more vectors when the Hamming distance between two successive vectors is unity.

A number of papers refer to *RobustH1* sequence as a robust test sequence [14], [16]–[18]. However in [3], it has been observed that *RobustH1* sequences are not necessarily robust. A robust test sequence is defined as follows [3]:

Definition 4: A *Robust test sequence* is a sequence of vectors that fulfills the following criteria:

1) The Hamming distance between two successive vectors should be unity.
2) During the application of test sequence, the sensitized path is free from any circuit glitches.

In the following discussion, we show that the *RobustH1* sequences may fail to detect a fault in the presence of glitches produced by timing skews/delay.

To illustrate the failure of *RobustH1* test sequences in the presence of glitches, consider the complex S-BJT BiCMOS gate shown in Fig. 6. If I is a pair of input vectors, that causes the output to change from 1 to 0, this is denoted by $I \Rightarrow (1, 0)$. Consider the fault when transistor P_2 is s-OPEN. To detect this fault, a test T is used, where $T = (t_1, t_2)$. Here, t_1 is the initialization vector, and t_2 is the test vector that sensitizes the fault. The initialization pattern t_1, in this example, is the one that initializes the output to logic "0"; it can be chosen from the following set of vectors:

$$t_1 = [001, 011, 101, 110, 111].$$

The second pattern t_2 is the actual test vector that sensitizes the fault P_2 s-OPEN, leading to $t_2 = [100]$.

To avoid the potential invalidation of the test sequence due to timing delays, a *RobustH1* test sequence that has unity Hamming distance between its patterns t_1 and t_2 can be chosen from the following set:

$$[ABC, \overline{ABC}] = [(101, 100), (110, 100)].$$

Let us first examine the sequence $T = (t_1, t_2) = (110, 100)$. The first pattern sets the output node to logic *ZERO,* and the second pattern creates the high impedance state in the presence of the fault, i.e., $T \Rightarrow (0, Z)$.

A negative glitch at node A caused by the prior logic during second pattern may turn ON the transistor P_1 momentarily, creating a low resistance path from output to V_{DD}. If the glitch is sufficiently wide, the output may charge causing the effect to appear as

$$T \Rightarrow (0, G_l, Z) \Rightarrow (0, 1).$$

Consequently, the test sequence fails to detect the fault. Similarly, one can show the sequence (101, 100) may fail in the presence of glitches. This example shows that any possible *RobustH1* test sequence may be potentially invalidated. Further, it can be shown that the positive glitches may cause the failure of all possible *RobustH1* test sequences for s-OPEN faults in the n-part. The reason for the failure of a sequence is the presence of glitches that interfere with the high impedance state. Hence, the failure of a sequence is possible irrespective of the method used for initialization. Such failures are possible not only with two-pattern sequences, but also with multiple pattern sequences.

One possible way to avoid test invalidation is to use robust test sequences that satisfy Definition 4. However, the criteria under Definition 4 impose difficult limitations. The first criterion implies that in every sum-of-product expression, the primary implicant should have at least one essential 1Vx that is adjacent to a 0Vx. A typical circuit does not satisfy this criterion. By introducing redundancy in the circuit, this requirement can be satisfied. However, a redundant circuit cannot be tested for 100% fault coverage.

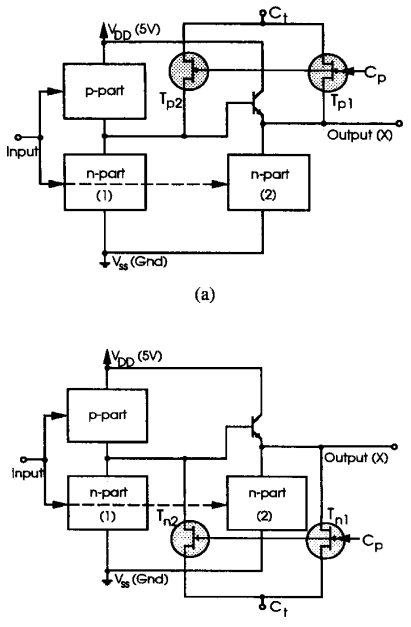

Fig. 7. Proposed testable design for testable BiCMOS gate using (a) pMOS DFT transistors and (b) nMOS DFT transistors.

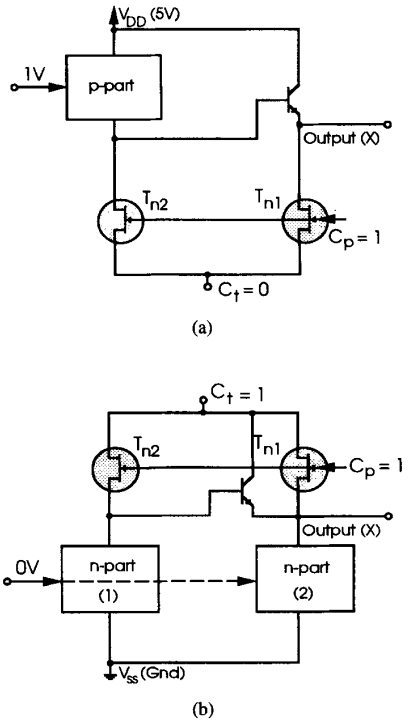

Fig. 8. Augmented BiCMOS gates during test mode using nMOS DFT transistors to test for s-OPEN faults in (a) p-part and BJT (b) n-parts.

The second criterion is even harder to satisfy. It implies that if (t_1, t_2) detects a s-OPEN fault in the p-part (n-part), the output of the gate under test should never become 1(0) due to a glitch. As mentioned above, glitches may occur due to various reasons. To identify all glitches and redesign a circuit to avoid them would be impossible.

Because of these limitations, obtaining robust test sequences that satisfy Definition 4 for all s-OPEN faults is impossible. To overcome this problem, we propose a testable design in the next section.

V. Design of Robust Testable BiCMOS Logic Gates

Behavior of S-BJT BiCMOS NAND and complex gate under s-OPEN failures were summarized in Section III. The two main observations are sequential behavior and delay faults. CMOS gates exhibit purely sequential behavior under s-OPEN failures, whereas single BJT BiCMOS devices exhibit delay faults also in addition to sequential behavior. Detection of s-OPEN faults exhibiting sequential behavior requires two-pattern or multipattern sequences. Delay faults are more difficult to test as the steady state value under fault-free and faulty conditions can be the same.

The proposed testable design ensures detection of s-OPEN faults using only one test vector and avoids using multipattern sequences or generating tests for delay faults. The proposed scheme allows testing the n-parts and the combination of p-part and bipolar separately, thus facilitating the use of a single test vector to detect s-OPEN fault. Instead of forcing the output to a high-impedance state to test for s-OPEN sequential behavior or detecting delay fault, the output node is connected to the power supply (ground) during the testing of n-parts (p-part and bipolar) through a resistance that is significantly higher than the ON resistances of the n- or p-parts.

Since the n-parts and the combination of p-part and bipolar are complementary to each other, when a vector turns the n-part ON, the combination of p-part and bipolar are turned OFF and vice-versa. The proposed testable design uses two DFT transistors, either two pMOS transistors or two nMOS transistors can be used as shown in Fig. 7(a) and (b). Each of the transistor is connected to the CMOS output of the BiCMOS device (base of the bipolar transistor) and at the output of the BiCMOS device (emitter of the bipolar transistor). The switching of the pass transistors are controlled by an external signal C_p, and the value passed is provided externally by the signal C_t. Two external control signals (C_p and C_t) and two p- or n-transistors are used in the proposed design as shown in Fig. 7(a) and (b).

Fig. 8 shows the conversion of the gate during the test mode. It should be noted that in Fig. 8(a) and (b), nMOS transistors are used, where all s-OPEN faults in the p-part and BJT (emitter or base open) can be tested by Fig. 8(a) and all s-OPEN faults in n-parts can be tested by Fig. 8(b). If nMOS transistors are used then during normal operation $C_p = 0$ and test mode $C_p = 1$. The same functionality can be obtained by pMOS transistors as shown in Fig. 9(a) and (b). If pMOS transistors are used, then during the normal operation $C_p = 1$, and during test mode $C_p = 0$. Table III summarizes the input vectors needed under normal and test modes with pMOS/nMOS transistors as DFT transistors.

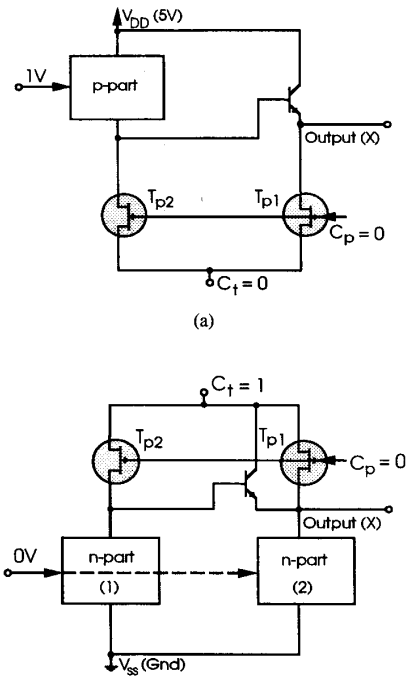

Fig. 9. Augmented BiCMOS gates during test mode using pMOS DFT transistors to test for s-OPEN faults in (a) p-part and BJT (b) n-parts.

TABLE III
SUMMARY OF INPUT VECTORS NEEDED UNDER NORMAL AND TEST CONDITIONS

Mode	Summary: pMOS DFT Transistors	Summary: nMOS DFT Transistors
	C_p C_t	C_p C_t
Normal Operation	1 X	0 X
Testing n-parts	0 1	1 1
Testing p-part	0 0	1 0

The extra transistors provide a static load at the output. The dimension of the extra transistors should be chosen such that the ON resistance of the transistors are considerably higher than the ON resistances of the p-part as well as the n-parts. With the use of pMOS transistor, for example, when $C_p = 0$, the gate is essentially transformed to a pseudo nMOS gate [25]. Therefore, the standard rules in designing pseudo nMOS (pseudo pMOS) type structures can be used to determine the size of the extra transistors. In general, a minimum size transistor, which offers a resistance of about 5–6 times higher than the ON resistance of the p- and n-parts are sufficient to provide the correct voltage levels.

Bipolar transistor (Q_1) emitter and base s-OPEN faults manifests as stuck-at-0 after initialization (shown as R in Table I). It can be seen that with either of the above faults, output cannot go to logic "1" (other than during power up) as no path exists between the output and V_{DD}. Detection of Q_1 emitter open and base open failures do not need any extra transistors as a test to detect stuck-at-0 at the output would detect these faults. However, with transistor Q_1 collector open, the output exhibits low-to-high transition delay ($D_{0\text{-}1}$) of approximately 2.4 ns instead of the normal 0.91 ns.

With the proposed augmentation, any s-OPEN fault can be detected by a single test vector. Results are formally stated as follows:

Theorem 1: By augmenting any single BJT BiCMOS gate as shown in Fig. 7, any single s-OPEN fault in the functional part can be detected by a single test vector. These tests are not invalidated by timing skews/delays, glitches, or charge sharing among the internal nodes.

Proof: The proof of this theorem is constructive. Consider a s-OPEN fault in either of the n-parts. The test vector for this fault is $C_pC_t = 11(01)$ with nMOS (pMOS) DFT transistors and a Zero Vertex (0Vx) covering the interested nMOS transistor. The 0Vx will turn the p-part and the bipolar OFF. Therefore, both parts of the augmented gate will appear as pull down n-part (1) and (2) and pull-up T_{n1}, $T_{n2}(T_{p1}, T_{p2})$ as shown in Figs. 8(b) or 9(b). If an s-OPEN fault is present in n-part (2), it will cause a high-resistance path between the output and ground resulting in logic ONE (1) at the output. If an s-OPEN fault is present in n-part (1), it will cause a high-resistance path between the base of the bipolar transistor and ground. With the application of 0Vx and with the DFT transistors (nMOS) (pMOS) turned ON, the base of the bipolar transistor would be at $[5\text{ V} - V_{th,n}]$ (5 V) which is greater than $V_{BE(cutin)}$ of the bipolar transistor, turning the bipolar transistor ON. $V_{th,n}$ is the threshold voltage of the nMOS DFT transistor. 0Vx turns the n-part (2) ON, but due to the wired-OR property [8] exhibited by the S-BJT device, output results in logic ONE (1). Hence, the output will appear to be at logic ONE (1) for both n-part (1) as well as n-part (2) s-OPEN failures. If the fault is not present, 0Vx will provide a low resistance path from bipolar transistor base to ground and output to ground. As the ON resistance of T_{p1}, $T_{p2}(T_{n1}, T_{n2})$ is considerably higher than the ON resistance of the n-part, the output will appear as logic ZERO (0). Therefore, a single test vector will detect the fault.

Similarly, consider an s-OPEN fault in the p-part. The test vector for this fault is $C_pC_t = 10$ (00) with nMOS (pMOS) DFT transistors, and a ONE Vertex (1Vx), covering the interested pMOS transistor. The 1Vx will turn the n-parts (1) and (2) OFF. Therefore, both parts of the augmented gate will appear as pull up p-part, bipolar transistor and pull down T_{n1}, $T_{n2}(T_{p1}, T_{p2})$ as shown in Figs. 8(a) or 9(a). If an s-OPEN fault is present in the p-part, there will be no conduction path from V_{DD} to the base of the bipolar transistor. With the application of 1Vx and with the DFT transistors nMOS (pMOS) turned ON, the base and emitter nodes of the bipolar transistor would be at 0 V ($V_{th,p}$), where $V_{th,p}$ is the threshold voltage of the pMOS DFT transistor. Therefore, $V_{BE} \approx 0$ V, and the bipolar transistor is OFF leading to logic "0" at the output. If the fault is not present, 1Vx will provide low resistance path from bipolar transistor base and output to V_{DD}. As the ON resistance of T_{p1}, $T_{p2}(T_{n1}, T_{n2})$ is considerably higher than the ON resistance of the p-part, the output will appear as logic ONE (1). Therefore, a single test vector will detect the fault. With bipolar transistor collector

open, there would still be a conduction path from V_{DD} to the output through the p-part and the base to emitter diode of the bipolar transistor and hence, this fault may not be detected.

The test vector brings the output node to a definite logic level and does not create a high impedance state. If a glitch appears during testing, although the output value may change momentarily, the steady-state will not be affected. The output voltage will recover after the glitch due to the path through T_{p1}, T_{p2} or T_{n1}, T_{n2}. Hence, the test cannot be invalidated because of timing skews/delays, glitches, or charge redistribution. In the unaugmented S-BJT BiCMOS designs, however, such a glitch could charge or discharge the output spuriously, and the output will not recover after the glitch because the second pattern creates a high-impedance state. Q.E.D

A first glance would lead one to expect the testable design to perform satisfactorily with just one DFT transistor (pMOS or nMOS) at the BiCMOS output. One DFT transistor at the BiCMOS output (Q_1 emitter output) would not work for testing either the p-part or n-part (1). For testing of n-part (1) s-OPEN faults, test vector $C_pC_t = 11(01)$ is applied with the nMOS (pMOS) DFT transistors and Zero Vertex (0Vx) covering the interested nMOS transistor. With the application of 0Vx and with just one DFT transistor (T_{p1} or T_{n1}) at the BiCMOS output turned ON, the output goes to logic "0," which does not detect the fault. By incorporating the second DFT transistor (T_{p2} or T_{n2}) at the base of the bipolar transistor enables the output to go to logic "1," which is opposite to the fault-free value, thus enabling detection of the fault. Similarly, consider using only one DFT transistor at the base of the bipolar transistor. While testing for s-OPEN fault in the n-part (1), the fault-free and faulty output would be logic "0," which does not detect the fault. Hence, both the transistors (T_{p1}, T_{p2} or T_{n1}, T_{n2}) are needed for the testable scheme to detect all s-OPEN faults successfully.

The following theorem can be directly deduced from the above Theorem 1.

Theorem 2: By augmenting any S-BJT BiCMOS gate as shown in Fig. 7, a test set that detects all single s-OPEN faults in the functional transistors will also detect all multiple s-OPEN faults in the functional part.

Proof: The complete test set for the augmented gate can be divided into two subsets. The first subset detects s-OPEN faults in n-parts (1) and (2) and the second subset detects s-OPEN faults in the p-part and bipolar. A test vector that detects a s-OPEN fault in n-part (1) also detects the corresponding s-OPEN fault in the n-part (2).

If the multiple s-OPEN faults in n-parts (1) and (2) involve the transistors corresponding to the same input, the test vector that detects s-OPEN fault in n-part (1) also detects the s-OPEN fault in n-part (2). Whereas, if the multiple s-OPEN faults in n-parts (1) and (2) do not involve the transistors corresponding to the same input, separate test vectors detect s-OPEN faults in n-parts (1) and (2) individually.

If the multiple s-OPEN faults involve transistors in n-parts (1) and (2) as well as p-part, separate test vectors detect s-OPEN faults in n-parts (1) and (2) as well as p-parts individually, thus, detecting the multiple s-OPEN faults.

A test vector for detection of s-OPEN faults switches off all the conduction paths and attempts to activate one conduction path from the output/base of bipolar to the ground (for testing of n-parts (1) and (2)), or the output/base of bipolar to the power supply (for testing of p-part and bipolar). This results in detection of all s-OPEN faults in that conduction path by this vector. If a multiple open fault involves two or more conduction paths, two or more vectors will be able to detect the fault. As we are considering s-OPEN faults, one fault cannot mask the effect of the other faults. Q.E.D

It is also interesting to see the efficiency of testing BiCMOS gate for a s-OPEN fault. The result is given as follows:

Theorem 3: The functional transistors in an augmented S-BJT BiCMOS gate, as shown in Fig. 7, can be tested for all single s-OPEN faults by a sequence of maximal length $2n$, where n is the number of transistors in the unaugmented BiCMOS n-part (1), n-part (2), or the p-part.

Proof: For testing the augmented gate for a s-OPEN fault, 0Vx (for n-part) or a 1Vx (for p-part) is applied. This 0Vx or 1Vx is chosen such that they cover the FET of interest. For the worst case, when only one FET is covered by a vector, we will need at most n test vectors to test one of the S-BJT BiCMOS p- or n-parts. Thus, to test the complete gate for all single s-OPEN faults, at most, $2n$ vectors are needed. Q.E.D.

It should be noted that the open faults in additional transistors cannot be tested in this design. However, an open fault in these transistors is benign and does not affect the normal circuit operation. Furthermore, single-fault assumption implies that the extra transistors are fault-free if a fault exists in the functional part and vice-versa.

Theorem 3 gives an upper bound for the length of the test sequence. In general, the length of the test sequence is much smaller. This is mainly due to the fact that a test vector examines the continuity of a path from the output to the power supply (V_{DD})/Ground.

An S-BJT BiCMOS gate is designed by addition of suitable bipolar and n-transistors for output driving purposes. An n-input CMOS gate uses $2n$ transistors, which is used in the BiCMOS gate to perform logic function. In addition, a bipolar transistor in conjunction with an n-part is used to drive output loads making the total number of transistors $(3n + 1)$. The bipolar transistor emitter and base s-OPEN failures can be detected by applying stuck-at-0 tests or the proposed testable design, and collector s-OPEN failure manifesting as low-to-high transition delay can be detected by the testable scheme. Hence, the number of functional transistors in an S-BJT BiCMOS gate that can be detected for s-OPEN faults using this scheme is $(3n + 1)$.

Power dissipation was computed for a BiCMOS NAND device with and without the implementation of the proposed testable design. The configuration shown in Fig. 3 was used to estimate the power dissipation. The power dissipation without the implementation of the proposed testable design for the configuration shown in Fig. 3 was computed to be $\approx$1.36 mW. Testable design was implemented for the BiCMOS NAND, and power computation was performed under fault-free and all possible single s-OPEN failure. The worst case power dissipation in the presence of a fault was computed to be $\approx$ 8.07 mW.

Hardware overhead of a BiCMOS device with the proposed testable design was estimated using a typical design rule. If the size of an nMOS transistor is $1n$ unit. The size of pMOS transistor is normally chosen to be 2 to 2.5 times of nMOS transistor resulting in $2.5n$ units. The size of BJT implementation is normally 3 to 4 times that of an nMOS transistor, resulting in a size of $4n$ units. The hardware overhead is higher when the testable design is implemented for primitive gates such as a 2-input NAND or NOR gate. The hardware overhead was computed and found to be 14% for a 2-input BiCMOS NAND device. The hardware overhead is much less when the testable design is implemented on complex BiCMOS devices as only 2 extra transistors are needed per gate to implement the testable design irrespective of the function being implemented.

An s-OPEN failure in the n-part (1), for example, N_1^{OP}/N_2^{OP} failures in NAND shown in Fig. 1, manifest as delay faults [8]. Tests for delay faults are much more difficult to generate. The proposed testable scheme avoids the requirement of generating tests for delay faults as the output is driven to logic "1."

VI. Advantages of the Proposed BiCMOS Testable Design

There are several advantages of the proposed S-BJT BiCMOS design. The most important advantage is that any s-OPEN fault can be detected by a single test vector. This reduces the testing time drastically. It reduces the test application time by 50% as it requires a single test vector instead of a sequence of two vectors or multipatterns. But more significant is the elimination of the test sequence generation. Complexity in generating two-pattern or multipattern sequences is a major cost factor in testing CMOS/BiCMOS s-OPEN faults. The complexity and cost associated with generating robust test sequences is even higher.

As only a single pattern is required to test for a given fault, the tests for the augmented gates can be generated by simple procedures. All the classical algorithms such as the D-algorithm, PODEM, and automatic test pattern generating programs (ATPG's) can generate the test for such augmented gates. The scheme detects the s-OPEN faults deterministically. Also, the proposed scheme offers significant advantage for random or pseudo-random testing procedures. Random testing is very inefficient for the detection of s-OPEN faults in FCMOS and S-BJT BiCMOS designs as the probability of fault detection depends on two successive vectors.

The proposed testable design requires a small amount of extra hardware for testing, which makes this design practical for actual implementation. Furthermore, since this scheme requires only an extra transistor at the base and emitter nodes of the bipolar transistor, the increase in the output capacitance is negligible. Also with the enhanced output drive and switching capability of the bipolar output, the delay caused due to the additional capacitance is negligible. A disadvantage in the proposed design is the slightly higher power dissipation during the testing. However, as this occurs only during testing, it is not a significant disadvantage.

VII. Conclusion

Physical failures causing transistor s-OPEN in a single BJT BiCMOS device were examined. In addition to sequential behavior observed in CMOS devices, BiCMOS devices also exhibit delay faults. Two-pattern or multipattern sequences are generally used to detect sequential behavior, and delay faults are much more difficult to detect. Two-pattern or multipattern sequences are difficult to obtain and may invalidate in the presence of glitches. The new testable design proposed in this paper uses only two additional transistors, uses only single vector instead of the two-pattern or multipattern sequences to detect any s-OPEN failures in the presence of timing skews/delays, glitches, or charge sharing among the internal nodes. The testable design scheme presented also avoids the requirement of generating tests for delay faults.

References

[1] A. R. Alvarez, *BiCMOS Technology and Applications.* Norwell, MA: Kluwer, 1989.

[2] B. C. Cole, "Is BiCMOS the next technology driver?" *Electron.,* pp. 55–57, Feb. 1988.

[3] R. Rajsuman, *Digital Hardware Testing: Transistor Level Fault Modeling and Testing.* Norwood, MA: Artech House, 1992.

[4] J. Gailiay, Y. Crouzet, and M. Vergniault, "Physical versus logical fault models in MOS LSI circuits: Impact on the testability," *IEEE Trans. Comput.,* vol. C-29, pp. 527–531, June 1980.

[5] Y. K. Malaiya, B. Gupta, A. P. Jayasumana, R. Rajsuman, S. M. Menon, and S. Yang, "Functional fault modeling for elementary static storage elements," Tech. Rep., Dept. Computer Science, Colorado State University, Apr. 1989.

[6] C. C. Beh, K. H. Arya, C. E. Radke, and K. E. Torku, "Do stuck fault models reflect manufacturing defects?" in *Proc. IEEE Test Conf.,* Nov. 1982, pp. 35–42.

[7] M. E. Levitt, K. Roy, and J. A. Abraham, "BiCMOS fault models: Is stuck-at adequate?" in *Proc. ICCD,* Sept. 1990, pp. 294–297.

[8] S. M. Menon, Y. K. Malaiya, and A. P. Jayasumana, "Behavior of faulty single BJT BiCMOS logic gates," in *Proc. 10th IEEE VLSI Test Symp.,* Apr. 1992, pp. 315–320.

[9] K. W. Chiang and Z. G. Vransic, "On fault detection in CMOS logic networks," in *Proc. 20th Des. Auto. Conf.,* June 1983, pp. 50–56.

[10] Y. K. Malaiya, A. P. Jayasumana, and R. Rajsuman, "A detailed examination of bridging faults," in *Proc. IEEE Int. Conf. Computer Design,* 1986, pp. 78–81.

[11] R. Rajsuman, Y. K. Malaiya, and A. P. Jayasumana, "On accuracy of switch-level modeling of bridging faults in complex gates," in *Proc. IEEE Design Automation Conf.,* 1987, pp. 244–250.

[12] Y. M. El-Ziq, "Automatic test generation for stuck-open faults in CMOS VLSI," in *Proc. 18th Des. Auto. Conf.,* June 1981, pp. 347–354.

[13] S. K. Jain and V. D. Agarwal, "Test generation for MOS circuits using D-algorithm," in *Proc. 20th Des. Auto. Conf.,* 1983, pp. 64–70.

[14] S. M. Reddy, M. K. Reddy, and J. G. Kuhl, "On testable design for CMOS logic circuits," in *Proc. Int. Test Conf.,* 1983, pp. 435–445.

[15] S. M. Reddy and M. K. Reddy, "Testable realization for FET stuck-open faults in CMOS combinational logic circuits," *IEEE Trans. Comput.,* vol. V-35, pp. 742–754, Aug. 1986.

[16] N. K. Jha and J. A. Abraham, "Design of testable CMOS logic circuits under arbitrary delays," *IEEE Trans. Computer-Aided Design,* vol. CAD-4, no. 3, pp. 264–469, July 1985.

[17] B. Gupta, Y. K. Malaiya, Y. Min, and R. Rajsuman, "On robust testable CMOS combinational circuits," in *IEE Proc. Part E,* July 1989, vol. 136, no. 4, pp. 329–338.

[18] D. L. Liu and E. J. McClusky, "Designing CMOS circuits for switch level testability," *IEEE Design Test,* vol. 4, no. 4, pp. 42–49, Aug. 1987.

[19] R. Rajsuman, A. P. Jayasumana, and Y. K. Malaiya, "CMOS open-fault detection in the presence of glitches and timing skews," *IEEE J. Solid-State Circuits,* pp. 1055–1061, Aug. 1989.

[20] A. P. Jayasumana, Y. K. Malaiya, and R. Rajsuman, "Design of CMOS circuits for stuck-open fault testability," *IEEE J. Solid-State Circuits,* vol. 26, no. 1, pp. 58–61, Jan. 1991.

[21] S. M. Menon, A. P. Jayasumana, and Y. K. Malaiya, "Testable design for detection of stuck-open faults in BiCMOS circuits using single patterns,"

Tech. Rep., Dept. Electr. Eng./Comput. Sci., Colorado State Univ., June 1992.
[22] *Fujitsu ECL & BiCMOS ASIC Selector Guide,* 1990, pp. 20–21.
[23] S. Chakravarty, "A characterization of robust test-pairs for stuck-open faults," *J. Electron. Test.: Theory Applicat.,* vol. 2, no. 1, pp. 275–286, Feb. 1991.
[24] S. Sastry and M. A. Breuer, "Detectability of CMOS stuck-open faults using random and pseudo random test sequences," *IEEE Trans. Computer-Aided Design,* vol. 7, pp. 933–946, Sept. 1988.
[25] N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design.* Reading, MA: Addison-Wesley, 1985, ch. 2.

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