Curriculum Vita

As of February 2018

Name	Sanjay V. Rajopadhye
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Education

1980 B.Tech. (Honors) Electrical Engineering, Indian Institute of Technology, Kharagpur, India.

1986 Ph.D. Computer Science, University of Utah, Salt Lake City, UT. (Dissertation: "Systolic Array Synthesis, Verification and Optimization")

Employment

1986–1991	Assistant Professor, Computer Science, University of Oregon.
1991–1992	Assistant Professor, Electrical and Computer Engineering, Oregon State University.
1992–94	Invited Researcher, IRISA / Professeur Associé, INSA, Rennes, France.
1994–04	Senior CNRS Researcher, IRISA, Rennes, France. Head of the COSI research group (Jan. 1997 – July 2004), on leave Sept. 2001 – July 2004
2001–	Computer Science, Colorado State University, Associate Professor, Full Professor since July 2013

Honors

- **As a student:** (i) National Science Talent Search (NSTS) Scholarship, India; (ii) Jagadis Bose National Science Talent Search Scholarship, 1975-1980; (iii) Fourth prize, second annual Utah VLSI design contest, 1983, and (iv) University of Utah Graduate Research Fellowship 1985-1986.
- NSF Research Initiation Award, 1988.
- Best presentation award, *Parcella '94:* International Workshop on Parallel Processing by Cellular Automata and Arrays, Potsdam, Germany, 1994.
- Best paper award, *IEEE* International Conference on Application Specific Array Processors, 1995.
- Finalist for best paper award, International Conference on Field Programmable Technology (FPT) 2010.

Grants and Contracts

- "Mechanical Synthesis of Systolic Arrays," NSF Research Initiation Award ($82k) 1988-1991.
- "A Prototype Scheduler for Parallel Processing Systems," (with V. Lo) Oregon Advanced Computing Institute (OACIS), ($68k) 1988-1989.
- "OREGAMI: Tools for mapping parallel algorithms to parallel architectures," (with V. Lo) OACIS, ($81k) 1989-1991.
- "Algorithms and Abstractions for Mapping Parallel Algorithms to Parallel Architectures" (with B. Bose and V. Lo), NSF and OACIS ($480k) 1992-1995.
- "Modélisation et Outils pour la Conception d'Architectures pour les Télécoms" (with F. Charot, P. Quinton and T. Risset), Région Bretagne (FF 250k), 1997-98.
- "CORCoP: Compilation and Optimisation for Reconfigurable Co-processors" Indo-French Centre for the Promotion of Advanced Research (FF 380k) 1999-2002.
- "SYSIL: Du Système au Silicium" project with STMicroelectronics, financed by the French Ministry of Industry(FF 340k), 1999.
- "HiPHiPECS: High Level Programming for High Performance Embedded Computing Systems" (with W. Böhm) NSF ($500k + $162k cost share) 2003.
- "ICAS: Itanium Compilation and Architecture Studies" (with W. Böhm, V. Chandrashekhar and A. Jayasumana) HP Philanthropy ($76k equipment grant) 2003.
- "Reconfigurable Coprocessor chips" Xilinx Inc., ($10k) Virtex II chips.
- "Meting the Need for Premises and Animal Identification Traceback," (with P. Burns) Colorado Department of Agriculture ($336k) 2005.
- "The Reduction Simplification Engine," NSF ($60k) 2008-09.
- "Simplifying Reductions" NSF, plus REU and International Supplements ($466k + $52k) 2009-12.
- "Evaluating the Computational Soundness and Enabling the Coarse Grained Parallelization of the NAADSM Epidemiological Simulation Model" USDA ($87k) 2009-10 (with PI Pallikara and co-PI Böhm).
- "Enabling Scalable and Fault Tolerant Regional Simulations in the Cloud" DHS ($738k) 2010-12 (with PI Pallikara and co-PI Böhm).
- "Open Source Compilation Tools for GPUs" Pathscale Inc., ($30k) 20010-11.
- "Co-design for Exascale GPGPU: Architecture, Programming, Tools, and Apps," NSF ($100k) 2012-2013.

- "Amorphous Polyhedral Model for Stochastic Control of Autonomous UAVs," AFOSR ($1M) 2013-2016.
- "Scalable Compilier Technology for Exascale," DoE ($300k) 2015-2016.

Professional Activities

- General/Program co-Chair, 2014 International Workshop on Polyhedral Compilation Techniques (IMPACT 2014).
- General/Program co-Chair, 2011 International Workshop on Languages and Compilers for Parallel Computing (LCPC).
- General co-Chair, 2006 IEEE International Conference on Application Specific Systems Architectures and Processors.
- Program co-Chair, 2006 IEEE/ACM International Conference on High Performance Computing.
- Program co-Chair, 2005 IEEE International Conference on Application Specific Systems Architectures and Processors.
- Program co-Chair, 2004 IEEE International Conference on Application Specific Systems Architectures and Processors.
- Program Committees
  - ERSA: International Conference on Engineering of Reconfigurable Systems and Algorithms (2005, 2006).
  - 2005 EUC: IFIP International Conference on Embedded and Ubiquitous Computing, Nagasaki, Japan.
  - Program IEEE International Conference on Application Specific Array Processing, 1994, 1995, 1996, 1997, 2000, 2006, 2007, 2008, 2009, 2010, 2111, 2012, 2014, 2015.
  - IEEE International Conference on High Performance Computing, 1996
  - IEEE International Conference on High Performance Computing, 1996
  - Rencontres Francophone sur le Parallélisme (Renpar) 1998, 1999, 2000, 2001.
  - International Workshop on Languages and Compilers for Parallel Computing (LCPC) 2010, 2012, 2013.
  - International Workshop on Polyhedral Compilation Techniques (IMPACT) 2011, 2012, 2013, 2015, 2015, 2016, 2018.
  - International Parallel and Distributed Processing Symposium 2005, 2013, 2014.
  - Conference on Languages, Compilers and Tools for Embedded Systems (LCTES 2013).

  - Workshop on Advances in Parallel and Distributed Computational Models, Associated with IPDPS (APDCM, 2013, 2014)
  - ACM/IEEE The International Conference for High Performance Computing, Networking, Storage and Analysis (Supercomputing) 20016, 2017, 2018.
  - International Conference on Compiler Construction (CC) 2016.
  - International Conference on Parallel Architectures and Compilation Techniques (PACT) 2017.

- External Review Committee:
  - PLDI: ACM International Conference on Programming Languages, Design & Implementation: 2011.
  - PPoPP: ACM International Conference on Principles and Practice of Parallel Programming: 2012, 2014.
  - International Symposium on Applied Reconfigurable Computing (ARC 2013).

- Co organiser, "International Seminar on Tiling for Optimal Resource Utilization", Dagstuhl, Germany, Aug 1998.
- Referee/Reviewer for IEEE Transactions on (i) Circuits and Systems, (ii) Computers, (iii) Computers Aided Design of Integrated Circuits and Systems, (iv) Acoustics, Speech and Signal Processing, (v) Parallel and Distributed Systems; Proceedings of IEEE, Journal of Parallel and Distributed Computing, Journal of VLSI Signal Processing, International Journal of Parallel Programming, Acta Informatica, Parallel Computing, IEEE Computer, ACM TOPLAS, ACM TACO.

Patents and Disclosures

- **Parallelization of Profile Hidden Markov Model Computations** disclosure filed September 2007.
- **Switched Memory Architectures:** (with G. Gupta and L. Renganarayana) issued August 2008, US 7,412,586 B1.

Open Source Software

- `Polylib:` A library for polyhedral operations (Doran Wilde: MS thesis under my supervision). IRISA, Rennes, 1994.
- `MMAlpha:` A tool for VLSI Array design, IRISA, Rennes, 1996.
- `AlphaZ:` A system for polyhedral program transformations, CSU 2010.

Publications

Books and Conference/Workshop Proceedings:

[B.1] **iHPerf 2000: Applications Parallèles Hautes Performances: Analyse, Conception et Utilisation de Grappes Homogènes ou Hétérogènes de Calculateurs** (co-editors: J-L. Pazat and J. Roman), Dec 2000, Aussois, France (French winter school on high performance computing).

Refereed Journals:

[J.1] **Formal Semantics for a Symbolic IC Design Technique: Examples and Applications** (with P. A. Subrahmanyam) *INTEGRATION: The VLSI Journal*, March 1985.

[J.2] **Synthesizing Systolic Arrays with Control Signals from Recurrence Equations**, *Distributed Computing*, May 1989.

[J.3] **Synthesizing Systolic Arrays from Recurrence Equations** (with R. M. Fujimoto), *Parallel Computing*, vol. 14, June 1990.

[J.4] **Automating the Design of Systolic Arrays** (with R. M. Fujimoto), *INTEGRATION: the VLSI Journal*, vol. 9, 1990.

[J.5] **Systolic Arrays for LU-Decomposition: An Application of Formal Techniques,** *International Journal of Computer Aided VLSI Design*, vol. 3, Jan 1991.

[J.6] **OREGAMI: Software Tools for Mapping Parallel Algorithms to Parallel Architectures** (with V. Lo, S. Gupta, D. Keldsen, M. Mohamed and J. Telle), *International Journal of Parallel Programming*, vol. 20, June 1991.

[J.7] **Quasi-Linear Allocation Functions for Efficient Array Design** (with X. Zhong) *Journal of VLSI Signal Processing*, Kluwer Academic Press, vol. 4, 1992.

[J.8] **Systematic Generation of Linear Allocation Functions in Systolic Array Design**, (with X. Zhong and I. Wong), *Journal of VLSI Signal Processing*, Kluwer Academic Press, vol. 4, 1992.

[J.9] **An Improved Systolic Algorithm for the Algebraic Path Problem**, *INTEGRATION: the VLSI Journal*, North Holland, vol. 14, Feb 1993.

[J.10] **A Shift Register Based Linear Systolic Array for the General Knapsack Problem** (with R. Andonov, P. Quinton and D. Wilde), *Parallel Processing Letters*, Feb 1995.

[J.11] **Parallel Divide and Conquer on Meshes** (with V. Lo, J. Telle and X. Zhong), *IEEE Transactions on Parallel and Distributed Systems*, vol 7, Oct 1996.

[J.12] **Multirate VLSI Arrays and their Synthesis** (with P. Lenders) *IEEE Transactions on Computers*, May 1997.

[J.13] **Knapsack on VLSI: from Algorithm to Optimal Circuit** (with R. Andonov), *IEEE Transactions on Parallel and Distributed Systems*, June 1997.

[J.14] **On Manipulating $\mathcal{Z}$-polyhedra using a Canonical Representation** (with P. Quinton and T. Risset), *Parallel Processing Letters*, June 1997.

[J.15] **Optimal Orthogonal Tiling of 2-D Iterations** (with R. Andonov) *Journal of Parallel and Distributed Computing*, Sept 1997.

[J.16] **Memory Reuse Analysis in the Polyhedral Model** (with D. Wilde) *Parallel Processing Letters*, June 1997.

[J.17] **Projet CAIRN: conception d'architectures à partir de Signal et Alpha** (with T. Gautier, P. Le Guernic, P. Quinton, T. Risset and I. Smarandache) *Collection Technique et Scientifique des Télécommunications*, Eyrolles, 1998, ch. 5.

[J.18] **Unbounded Knapsack Problem: Dynamic Programming Revisited** (with R. Andonov and V. Poirriez), in *European Journal of Operations Research* (June 2000).

[J.19] **Generation of Efficient Nested Loops from Polyhedra** (with F. Quilleré and D. Wilde), in *IJPP: International Journal of Parallel Programming,* (October 2000).

[J.20] **Derivation Of Systolic Algorithms For The Algebraic Path Problem By Recurrence Transformations** (with C. Tayou Djamegni, P. Quinton and T. Risset), in *Parallel Computing* (October 2000).

[J.21] **Optimizing Memory Usage in the Polyhedral Model** (with F. Quilleré) in *ACM TOPLAS: Transactions on Programming Languages and Systems,* (September 2001).

[J.22] **Le Chemin Algébrique sur Réseaux Linéaires** (with T. Risset and C. Tadonki), in *Technique et Sciences Informatiques* May 2001.

[J.23] **Optimal Semi-Oblique Tiling** (with R. Andonov, S. Balev and N. Yanev), in *IEEE Transactions on Parallel and Distributed Systems*, Sept 2003.

[J.24] **Development of computational models for the purpose of collecting individual livestock and premises traceback investigations utilizing National Animal Identification System-compliant data** (with J. A. Scanga, T. Hoffman, J. Picanso, D.G. Kim, A. Gupta, R. Forbes, J. Ladd and P. Burns), in *Journal of Animal Sciences*, vol. 85 2006.

[J.25] **A reindexing based approach towards mapping of DAG with affine schedules onto parallel embedded systems** (with C. Tayou-Djamegni, P. Quinton, T. Risset and M. Tchuente), in *Journal of Parallel and Distributed Computing*, (2009).

[J.26] **Parameterized Loop Tiling** (with L. Renganarayana, DG. Kim and M. Strout), *ACM TOPLAS: Transactions of Programming Languages and Systems,* (2012).

[J.27] **Bridging the Chasm Between MDE and the World of Compilation** (with J-M. Jézéquel, B. Combemale, S. Derrien, and C. Guy) *Software and Systems Modeling*, Springer, (2012).

[J.28] **Improving Reliability of Islanded Distribution Systems With Distributed Renewable Energy Resources** (with H. E. Brown, S. Suryanarayanan, and S. Natarajan). IEEE Trans. Smart Grid 3(4): 2028-2038 (2012).

[J.29] **Optimizing Dynamic Resource Allocation** (with L. Krakow, L. Rabiet, Y. Zou, G. Iooss and E. K. P. Chong) in *Procedia Computer Science*, Elsevier 2014.

[J.30] **Combining Execution Pipelines to Improve Parallel Implementation of HMMER on FPGA** (with N. Abbas, S. Derrien, P. Quinton, A. Cornu and D. Lavenier), *Microprocessors and Microsystems*, 37(7), 2015.

[J.31] **A Code Generator for Energy-Efficient Wavefront Parallelization of Uniform Dependence Computations** (with Yun Zou) *IEEE Transactions on Parallel and Distributed Systems*, 2017 (in press).

Book Chapters:

[BC.1] [invited] **Systematic Derivation of VLSI Arrays for Digital Filters** (with S. Kiaei), in *Advances in VLSI Signal Processing*, Ed. M. Bayoumi 1991.

[BC.2] [invited] **Affine Permutations of Matrices on Mesh Connected Arrays** (with B. Lisper), in *Parallel Algorithms and Architectures for DSP Applications*, Ed. M. Bayoumi, Kluwer Academic Press, 1991.

[BC.3] [invited] **Advanced Systolic Design** (with D. Lavenier and P. Quinton), in *Digital Signal Processing for Multimedia Systems*, Eds. K. Parhi and T. Nishitani, Marcel Dekker, 1999.

[BC.4] [invited] **Dependence Analysis and Parallelizing Transformations**, *Handbook on Compiler Design*, Eds. Priti Shankar and Y. N. Srikant, CRC Press (2002).

[BC.5] **Back Propagation Algorithm: Achieving 5 GOPS on the Virtex-E** (with K. Paul), book chapter in *FPGA Implementations of Neural Nets*, Kluwer Academic (2006).

[BC.6] [invited] **Computations on Iteration Spaces**, *Handbook on Compiler Design, Second Edition*, (with G. Gupta, L. Renganarayana and M. Strout) Eds. Priti Shankar and Y. N. Srikant, CRC Press (2007).

[BC.7] [invited] **High-Level Synthesis of loops using the Polyhedral Model**, (with S. Derrien, P. Quinton and T. Risset) *High-Level Synthesis from Algorithm to Digital Circuit*, Eds. P. Coussy and A. Morawiec (2008).

[BC.8] **GPU accelerated RNA folding algorithm**, *GPU Computing Gems 4*, (with G. Rizk and D. Lavenier) Editor in Chief W-M. Hwu, Addison Wesley, Ch 14, 2010.

Refereed/Invited Conferences and Workshops:

[RC.1] **Formal Semantics for a Symbolic IC Design Technique** (with P. A. Subrahmanyam), in *International Conference on Circuit Design*, Oct 1983, Rye, NY.

[RC.2] **Verification of Systolic Arrays: A Stream Functional Approach** (with P. Panangaden), in *IEEE-ACM International Conference on Parallel Processing*, Aug 1986, St. Charles, IL.

[RC.3] **On Synthesizing Systolic Arrays from Recurrence Equations with Linear Dependencies** (with S. Purushothaman and R. M. Fujimoto), in *Foundations of Software Technology and Theoretical Computer Science*, Dec 1986, New Delhi, India, Springer Verlag LNCS.

[RC.4] **Systolic Array Synthesis by Static Analysis of Program Dependencies** (with R. M. Fujimoto), in *PARLE 87: Parallel Architectures and Languages Europe*, June 1987, Eindhoven, the Netherlands, Springer Verlag LNCS.

[RC.5] **I/O Behavior of Systolic Arrays**, in *IEEE Workshop on VLSI Signal Processing*, Nov 1988, Monterey, CA.

[RC.6] **Algebraic Transformations in Systolic Array Synthesis: A Case Study**, in *IFIP International Workshop on Applied Formal Methods for Correct VLSI Design*, Nov 1989, Leuven, Belgium.

[RC.7] [invited] **Matrix Permutations on Mesh-Connected Arrays** (with B. Lisper), in *IEEE International Symposium on Circuits and Systems*, May 1990, New Orleans, LA.

[RC.8] **OREGAMI: Software Tools for Mapping Parallel Algorithms to Parallel Architectures** (with V. Lo, S. Gupta, D. Keldsen, M. Mohamed and J. Telle), in *IEEE-ACM International Conference on Parallel Processing*, Aug 1990, St. Charles IL.

[RC.9] **Mapping Divide and Conquer Algorithms to Parallel Architectures**, (with V. Lo, S. Gupta, D. Keldsen, M. Mohamed and J. Telle), in *IEEE-ACM International Conference on Parallel Processing*, Aug 1990, St. Charles IL.

[RC.10] **Scheduling Affine Parameterized Recurrences by means of Variable Dependent Timing Functions** (with C. Mauras, P. Quinton and Y. Saouter), in *IEEE International Conference on Application Specific Array Processors*, Princeton, NJ, Sept 1990.

[RC.11] **Bounds on the Number of Linear Allocation Functions** (with I. Wong and X. Zhong), in *IEEE Workshop on VLSI Signal Processing*, San Diego, CA, Nov 1990.

[RC.12] [invited] **An Improved Systolic Algorithm for the Algebraic Path Problem**, in *Algorithms and Parallel VLSI Architectures II*, Bonas, France, June 1991.

[RC.13] **Deriving Fully Efficient Systolic Arrays by Quasi-Linear Allocation Functions** (with X. Zhong) in *PARLE 91: Parallel Architectures and Languages Europe*, Eindhoven, the Netherlands, June 1991, Springer Verlag LNCS.

[RC.14] **Reasoning About Permutations in Regular Arrays** (with B. Lisper) in *IFIP Workshop on Designing Correct Circuits*, Lyngby, Denmark, Jan 1992, Springer Verlag LNCS.

[RC.15] **Mapping parallel divide and conquer algorithms to binary de-Bruijn networks** (with X. Zhong and V. Lo), in *IEEE-ACM International Parallel Processing Symposium*, Beverly Hills, CA March 1992.

[RC.16] **Piecewise Linear Schedules for Recurrence Equations** (with L. Mui and S. Kiaei), in *IEEE Workshop on VLSI Signal Processing, V*, Napa, CA Oct 1992.

[RC.17] [invited] **LACS: A Language for Affine Communication Structures**, in *Seminar on Parallelization Techniques for Uniform Algorithms*, Dagstuhl, Germany, June 1993.

[RC.18] **An Optimal Algo-tech-cuit for the Knapsack Problem**, (with R. Andonov) in *ASAP93: IEEE International Conference on Application Specific Array Processing*, Venice, Italy, Oct 1993.

[RC.19] **Analysis of Affine Communication Specifications**, in *IEEE Symposium on Parallel and Distributed Processing*, Dallas TX, Dec 1993.

[RC.20] **Des graphes de flots de données synchrones pour le VLSI** (with A. Kerihuel et R. McConnell), in *RENPAR 6: Rencontres francophones du parallélisme*, Lyon, France, June 1994.

[RC.21] **A Sparse Knapsack Algo-tech-cuit and its Synthesis**, (with R. Andonov), in *ASAP 94: IEEE International Conference on Application Specific Array Processing Conference*, San Francisco, CA, Aug 1994.

[RC.22] **Optimal Tiling** (with R. Andonov), in *CONPAR 94*, Linz, Austria, September 1994.

[RC.23] **Pure Systolic Array for a Class of Recurrences with Dynamic Dependencies**, (with R. Andonov, P. Quinton and D. Wilde), in *PARCELLA 94*, Potsdam, Germany, Sept 1994.

[RC.24] **What is a Multirate Array?** (with P. Lenders), in *IEEE Workshop on VLSI Signal Processing*, La Jolla, CA, Oct 1994.

[RC.25] **Derivation of Data Parallel Code from a Functional Program** (with P. Quinton and D. Wilde), in *IEEE International Parallel Processing Symposium*, Santa Barbara, CA, April 1995.

[RC.26] **Deriving Imperative Code from Functional Programs** (with P. Quinton and D. Wilde), in *ACM FPCA: Conference on Functional Programming and Computer Architecture*, La Jolla, CA, June 1995.

[RC.27] **Synthesis of Multirate VLSI Arrays** (with P. Lenders), in *IEEE Conference on Application Specific Array Processors*, Strasbourg, France, July 1995.

[RC.28] **The Naive Execution of Affine Recurrence Equations** (with D. Wilde), in *IEEE Conference on Application Specific Array Processors*, Strasbourg, France, July 1995.

[RC.29] **A Regular VLSI Array for an Irregular Algorithm** (with F. de Dinechin, D. Wilde and R. Andonov), in *Irregular 96: Third International Workshop on Parallel Algorithms for Irregularly Structured Problems*, Santa Barbara, Aug 1996.

[RC.30] **Extension of the Alpha language to recurrences on sparse periodic domains** (with P. Quinton and T. Risset), in *IEEE Conference on Application Specific Systems Architectures and Processors*, Chicago, IL, Aug 1996.

[RC.31] **Memory Reuse Analysis in the Polyhedral Model** (with D. Wilde), in *Europar 96: Parallel Processing Conference*, Lyon, France, Aug 1996.

[RC.32] **Two-dimensional Orthogonal Tiling: from Theory to Practice** (with R. Andonov and H. Bourzoufi) in *IEEE International Conference on High Performance Computing*, Trivandrum, India, Dec 1996.

[RC.33] **Linear Programming Models for Scheduling Systems of Affine Recurrence Equations: A Comparative Study** (with S. Balev, P. Quinton and T. Risset), in *SPAA-98: Tenth ACM Symposium on Parallel Algorithms and Architectures*, Puerto Vallarta, Mexico, June-July 1998.

[RC.34] **Optimal Orthogonal Tiling**, (with R. Andonov and N. Yanev) in *Fourth International Euro-Par Conference*, Southampton, UK, Sept 1998.

[RC.35] **The Algebraic Path Problem Revisited** (with C. Tadonki and T. Risset) in *Fifth International Euro-Par Conference*, Toulouse, France, Aug-Sept 1999.

[RC.36] **Quadratic Control Signals in Linear Systolic Arrays**, (with S. Bowden and D. Wilde), in *ASAP 2000: IEEE International Conference on Application Specific Array Processing*, Boston, MA, July 2000.

[RC.37] **Custom Computing and the Memory Wall**, (with S. Derrien), in *FCCM 2000: IEEE Symposium on Field-Programmable Custom Computing Machines*, Napa, CA, April 2000.

[RC.38] **First Steps Towards Optimal Oblique Tile Sizing,** (with R. Andonov, P-Y. Calland, S. Niar and N. Yanev,) in *8th International Workshop on Compilers for Parallel Computers,*, 2000.

[RC.39] **Optimal Semi-Oblique Tiling** (with R. Andonov, S. Balev and N. Yanev), in *SPAA 2001: Thirteenth ACM Symposium on Parallel Algorithms and Architectures*, July 2001, Crete.

[RC.40] **Proving Properties of Multidimensional Recurrences with Applications to Regular Parallel Algorithms** (with D. Cachera, P. Quinton and T. Risset), in *FMPPTA*

2001: 6th International Workshop on Formal Methods for Parallel Programming: Theory and Applications, April 2001, San Francisco, CA.

[RC.41] **Combined Instruction and Loop Parallelism in Array Synthesis for FPGAs** (with S. Derrien and S. Sur-Kolay), in *ISSS 2001: 14th International Symposium on System Synthesis*, September 2001, Montreal, Canada.

[RC.42] **Loop Tiling for Reconfigurable Accelerators** (with S. Derrien), in *FPL 2001: International Conference on Field-Programmable Logic*, August 2001, Belfast, Ireland.

[RC.43] **Uniformization of Affine Dependence Programs for Parallel Embedded System Design** (with M. Manjunathaiah, G. M. Megson, and T. Risset), in *ICPP 2001: 30th International Conference on Parallel Processing*, September 2001, Valencia, Spain.

[RC.44] **Scheduling Reductions on Realistic Machines** (with G. Gupta and P. Quinton), in *SPAA 2002: Fourteenth ACM Symposium on Parallel Algorithms and Architectures,* August 2002, Winnipeg, Canada.

[RC.45] **Energy/Power Estimation of Regular Processor Arrays** (with S. Derrien), in *ISSS 2002: 15th International Symposium on System Synthesis*, October 2002, Kyoto, Japan.

[RC.46] **Switched Memory Architectures: Moving Beyond Systolic Arrays** (with L. Renganarayana), in *ASAP 2003: International Conference on Application Specific Systems Architectures and Processors*, June 2003, den Hague, Netherlands.

[RC.47] [invited] **Dynamically Switched Interconnect for SoC's**, in *Seminar on Dynamically Reconfigurable Architectures*, Dagstuhl, Germany, July 2003.

[RC.48] **A Geometric Programming Framework for Optimal Multi-level Tiling**, (with L. Renganarayana) in *Supercomputing* 2004, Pittsburgh PA.

[RC.49] **A 1.5D Architecture for Back Propagation Training**, (with K. Paul) in *ERSA 2005: Engineering of Reconfigurable Systems and Algorithms* 2005, Las Vegas, NV.

[RC.50] **Combined ILP and Register Tiling: Analytical Model and Optimization Framework**, (with L. Renganarayana and U. Ramakrishna) in *LCPC 2005: International Workshop on Languages and Compilers for Parallel Computing* 2005, Hawthorne, NY.

[RC.51] **Simplifying Reductions**, (with Gautam) in *POPL 2006: ACM Symposium on Principles of Programming Languages* 2006, Charleston, SC.

[RC.52] **An Improved Systolic Architecture for LU Decomposition**, (with D.G. Kim) in *ASAP 2006: IEEE International Conference on Application Specific Systems Architectures and Processors* 2006, Steamboat Springs, CO.

[RC.53] **On Control Signals for Multidimensional Time**, (with D.G. Kim and Gautam) in *LCPC 2006: International Workshop on Languages and Compilers for Parallel Computing* 2006, New Orleans, LA.

[RC.54] **The $\mathcal{Z}$-Polyhedral Model**, (with Gautam) in *PPoPP 2007: ACM Symposium on Principles and Practices of Parallel Programming* 2007, San Jose, CA.

[RC.55] **Scheduling in the $\mathcal{Z}$-Polyhedral Model**, (with Gautam and D.G. Kim) in *IPDPS 2007: IEEE International Parallel and Distributed Processing Symposium* 2007, Long Beach, CA.

[RC.56] **Towards Optimal Multi-level Tiling for Stencil Computations**, (with L. Renganarayana, M. Harthikote and R. Dewri) in *IPDPS 2007: IEEE International Parallel and Distributed Processing Symposium* 2007, Long Beach, CA.

[RC.57] **Parameterized Tiled Loop Generation for Free**, (with L. Renganarayana, D.G. Kim and M. Strout) in *PLDI 2007: ACM Symposium on Principles and Practices of Parallel Programming* 2007, San Diego, CA.

[RC.58] **Multi-level Tiling: m for the Price of One**, (with L. Renganarayana, D.G. Kim and M. Strout) in *Supercomputing* 2007, Reno NV.

[RC.59] **0/1 Knapsack on Hardware: A Complete Solution**, (with K. Nibbelink and R. McConnell), in *ASAP 2007: 18th IEEE International Conference on Application-specific Systems, Architectures and Processors* Montréal, Québec, Canada.

[RC.60] [invited] GRAIL: **A Generic Reconfigurable Affine Interconnection Lattice**, (with Gautam and L. Renganarayana) Dagstuhl, Germany 2007.

[RC.61] **A Domain Specific Interconnect for Reconfigurable Computing**, (with Gautam and L. Renganarayana) *LCTES 2008: ACM Conference on Languages, Compilers, and Tools for Embedded Systems* 2008, Tucson, AZ.

[RC.62] **Smashing: Folding Space to Tile Through Time** (with N. Osheim, M. Strout and D. Rostrom) *LCPC 2008: 15th Workshop on Languages and Compilers for Parallel Computing.*

[RC.63] **Positivity, Posynomials, and Tile Size Selection**, (with L. Renganarayana) in *SC 2008: ACM/IEEE conference on Supercomputing* 2008, Austin, TX.

[RC.64] **Efficient Tiled Loop Generation: D-Tiling**, (with D. Kim) in *LCPC 2009: 22nd International Workshop on Languages and Compilers for Parallel Computing* Newark, DE.

[RC.65] **Automatic creation of tile size selection models**, (with T. Yuki, L. Renganarayana, C. Anderson, A. E. Eichenberger, K. O'Brien) in *CGO 2010: ACM International Symposium on Code Generation and Optimization* 2010, Toronto, Canada.

[RC.66] **Accelerating HMMER on FPGA using Parallel Prefixes and Reductions**, (with N. Abbas, S. Derrien, and P. Quinton) in *FPT 2010: International Conference on Field-Programmable Technology*, 2010 Tsinghua, China (finalist for the best paper award).

[RC.67] **Alphabets: An Extended Polyhedral Equational Language**, (with G. Gupta, and D. Kim) in *13th Workshop on Advances in Parallel and Distributed Computational Models*, 2011 Anchorage, AK.

[RC.68] **Improving CUDASW++, a Parallelization of Smith-Waterman for CUDA Enabled Devices**, (with Z. Cachero, D. Hains, M. Ottenberg, and W. Böhm) to appear in *Tenth IEEE International Workshop on High Performance Computational Biology, HiCOMB* 2011, Anchorage, AK.

[RC.69] **ompVerify: Polyhedral Analysis for the OpenMP Programmer**, (with V. Basupalli, T. Yuki, Rajopadhye, A. Morvan, S. Derrien, P. Quinton, D. Wonnacott), in *IWOMP 2011: International Workshop on OpenMP*, 2011, Chicago IL.

[RC.70] **Model-Driven Engineering and Optimizing Compilers: A bridge too far?**, (with T. Yuki, A. Floch, S. Derrien, B. Combemale, R. France, C. Guy) in *MODELS 2011: ACM/IEEE 14th International Conference on Model Driven Engineering Languages and Systems*, Wellington New Zealand.

[RC.71] **A Library to Manipulate Z-polyhedra in Image Representation**, (with G. Iooss) in *IMPACT 2012: 2nd International Workshop on Polyhedral Compilation Techniques*, Paris, France.

[RC.72] **Scan Detection and Parallelization in "Inherently Sequential" Nested Loop Programs** (with Y. Zou), *CGO 2012: International Symposium on Code Generation and Optimization*, San Jose, CA.

[RC.73] **AlphaZ: A System for Design Space Exploration in the Polyhedral Model** (with T. Yuki, G. Gupta, DG. Kim, and T. Pathan), in *LCPC 2012: 25th Workshop on Languages and Compilers for Parallel Computing*, Tokyo, Japan.

[RC.74] **Memory Allocations for Tiled Uniform Dependence Programs** (with T. Yuki), in *3rd International Workshop on Polyhedral Compilation Techniques: IMPACT 2013*, Berlin, Germany.

[RC.75] **Array Dataflow Analysis for Polyhedral X10 Programs** (with T. Yuki, P. Feautrier and V. Saraswat) in *ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming: PPoPP 2013*, Shenzhen, China.

[RC.76] **Compilation of Structured Polyhedral Equations**, (with Y. Zou, and G. Iooss), in *CPC 2013: 17th Workshop on Compilers for Parallel Computing*, Lyon, France.

[RC.77] **Folklore Confirmed: Compiling for Speed = Compiling for Energy**, (with Tomofumi Yuki), in *LCPC 2013: International Workshop on Languages and Compilers for Parallel Computing.*

[RC.78] **CART: Constant Aspect Ratio Tiling** (with G. Iooss, C. Alias, and Y. Zou) in *IMPACT 2014: 4th International Workshop on Polyhedral Compilation Techniques*, Vienna, Austria.

[RC.79] **On Program Equivalence with Reductions**, (with G. Iooss and C. Alias) in *SAS 2014: 21st International Static Analysis Symposium*, Munich, Germany.

[RC.80] **Optimizing Dynamic Resource Allocation** (with L. Krakow, L. Rabiet, Y. Zou, G. Iooss and E. K. P. Chong) in *ICCS 2014: International Conference on Computational Science* Cairns, Australia.

[RC.81] **Automatic Energy Efficient Parallelization of Uniform Dependence Computations** (with Y. Zou) in *ACM ICS 2015: International Conference on Supercomputing* Newport Beach, CA.

[RC.82] **Energy Modeling and Optimization for Tiled Nested-Loop Codes**, (with N. Prajapati, W. Ranasinghe, V. Tandrapati, R. Andonov, and H. Djidjev) in *HP-PAC 2015: Workshop High-Performance, Power-Aware Computingq, in conjunction with IPDPS 2015*, Hyderabad, India.

[RC.83] **Towards Scalable and Efficient FPGA Stencil Accelerators**, (with G. Deest, N. Estibals, T. Yuki and S. Derrien) in *IMPACT 2016: 6th International Workshop on Polyhedral Compilation Techniques*, Prague, Czech Republic.

[RC.84] **Simple, Accurate, Analytical Time Modeling and Optimal Tile Size Selection for GPGPU Stencils**, (with N. Prajapati, W. Ranasinghe, R. Andonov, H. Djidjev, and T. Grosser) in *PPoPP 2017: 22nd ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, Austin TX.

[RC.85] **One size does not fit all: Implementation trade-offs for iterative stencil computations on FPGAs**, (with G. Deest, T. Yuki and S. Derrien) in *FPL 2007: 27th IEEE International Conference on Field Programmable Logic and Applications*, Ghent, Belgium.

Other Conferences/Workshops:

[OC.1] **Systolic Arrays for LU-Decomposition**, in *International Symposium on Circuits and Systems International Symposium on Circuits and Systems (ISCAS)*, June 1988, Espoo, Finland.

[OC.2] **User Interface Issues in CAD Tools for Systolic Array Design**, in *Midwest Symposium on Circuits and Systems*, Aug 1989, Urbana-Champaign, IL.

[OC.3] **Cost Measures in Systolic Array Design**, (with P. Cappello), in *Pacific Rim Conference on Circuits and Systems*, May 1991, Victoria, Canada.

[OC.4] **Synthesizing Efficient Systolic Arrays** (with X. Zhong), in *International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, Toronto, Canada, June 1991.

[OC.5] **A Folding Transformation for VLSI IIR Filter Array Design** (with S. Kiaei), in *International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, Toronto, Canada, June 1991.

[OC.6] **Parallel Assignment, Reduction and Communication** (with M. Muddarangegowda), in *SIAM Conference on Parallel Processing for Scientific Computing*, Norfolk, VA, March 1993.

[OC.7] **VSDF: Synchronous Data Flow for VLSI**, (with A. Kerihuel et R. McConnell), in *Midwest Symposium on Circuits and Systems*, Lafayette, LA, Aug 1994.

[OC.8] **Multiphase Multirate Arrays** (with P. Lenders), in *Australian .Computer Science Conference*, Adelaide, Australia, Feb 1995.

[OC.9] **Multirate and Sparse Systolic Architectures** (with N. Dunstan and P. Lenders), in *Australian Computer Architecture Workshop*, Melbourne, Australia, Jan 1996.

[OC.10] **Generating Regular Arithmetic Circuits with AlpHard** (with P. le Moenner, L. Perraudeau, P. Quinton and T. Risset), in *MPCS'96: Massively Parallel Computing Systems*, May 1996, Ischia, Italy.

[OC.11] **Localization of Algorithms for VLSI Implementation** (with P. Lenders), in *Parallel and Distributed Computing and Networks*, Brisbane, Australia, Dec 1998.

[OC.12] **Optimizing Memory Usage in the Polyhedral Model** (with F. Quilleré), in *MPCS'98: Massively Parallel Computing Systems*, April 1998, Colorado Springs, CO.

[OC.13] **Optimal Partitioning for FPGA based Regular Array Implementations** (with S. Derrien and S. Sur-Kolay), in *PARELEC 2000: IEEE Conference on Parallel Computing in Electrical Engineering*, August 2000, Trois Riviers, Quebec.

[OC.14] **Hardware Design Methodology with the Alpha Language** (with A-C. Guillou, F. Quilleré P. Quinton and T. Risset), in *FDL 01: Forum on Design Languages*, Sept 2001, Lyon, France.

[OC.15] **Alphabets: An Extended Polyhedral Equational Language**, (with G. Gupta, and D. Kim) in *23rd International Workshop on Languages and Compilers for Parallel Computing*, 2010 Houston, TX (poster).

[OC.16] **AlphaZ and the Polyhedral Equational Model**, (with T. Yuki) in *Second International Workshop on Domain-Specific Languages and High-Level Frameworks for High Performance Computing,* 2012.

[OC.17] **Semantic Tiling**, (with G. Iooss, and C. Alias) in *LASH-C 2013: Workshop on Leveraging Abstractions and Semantics in High-performance Computing, in conjunction with PPoPP 2013*, Shenzhen, China.

[OC.18] **Parallelizing Stencils Automatically for Energy**, (with Y. Zou) in *IMPACT 2015: 5th International Workshop on Polyhedral Compilation Techniques*, 2016 Amsterdam, the Netherlands (poster)

Graduate Students Supervised

Before coming to CSU

I. Wong	MS, University of Oregon, Dec 1989
L. Mui	MS, Oregon State University, Jan 1992
S. Srinivasan	MS, Oregon State University, Aug 1992
X. Zhong	PhD, University of Oregon, July 1994 (co-supervised with V. Lo)
D. Wilde	PhD, Oregon State University (July 1995)
F. de Dinechin	PhD, Université de Rennes, Jan 1997 (co-supervised with P. Quinton)
C. Tadonki	PhD, Université de Rennes (March 2001, co-supervised with B. Philippe, IRISA, Rennes and M. Tchuenté, University of Dchang, Cameroon)
S. Derrien	PhD, Université de Rennes (December 2002)

At CSU

V. Ukidve	MS (ECE, January 2004)
A. Sanyal	MS (CS, August 2005)
D.G. Kim	MS (CS, December 2005)
A. Gupta	MS (CS, May 2007)
U. Ramakrishna	MS (CS, May 2008)
N. Burnett	MS (CS, December 2008)
K. Nibbelink	MS (CS, May 2009)
T. Yuki	MS (CS, December 2009)
T. Pathan	MS (ECE, Deceber 2010)
P. Srinivasa	MS (CS, December 2010)
S. Sui	MS (CS, December 2010)
V. Basupalli	MS (CS, September 2011)
Y. Zou	MS (CS, September 2011)
L. Rabiet	MS (Université de Rennes I, September 2013)
V. Tandrapati	MS (ECE, December 2014)
W. Ranasinghe	MS (CS, December 2014)
M. Puranik	MS (ECE, Fall 2015)
R. Rajasree	MS (ECE, July 2016)
R. Chandramohan	MS (ECE, Dec 2016)
S. Varadarajan	MS (ECE, Oct 2017)
R. Lakshminarayanan	PhD, CSU (May 2008)
G. Gupta	PhD (CS, June 2010)
D.G. Kim	PhD (CS, April 2010)
G. Rizk	PhD, Univ. Rennes (January 2011) co-supervisor D. Lavenier
T. Yuki	PhD (CS, December 2012)
Y. Zou	PhD (CS, June 2016)
G. Iooss	PhD (CS, July 2016) co-supervisor C. Alias
N. Prajapati	PhD (CS, ongoing since Jan 2012)
W. Ranasinghe	PhD (CS, ongoing since Aug 2012)
S. Varadarajan	PhD (CS, ongoing since Jan 2018)
P. Ghalsasi	MS (ECE, ongoing since Aug 2015)
T. Sifat	MS (CS, ongoing since Aug 2017)